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CEDFPD board

Board in VXI format which realize the coincidence between the CED and THE FPD detectors for the G0 experiment

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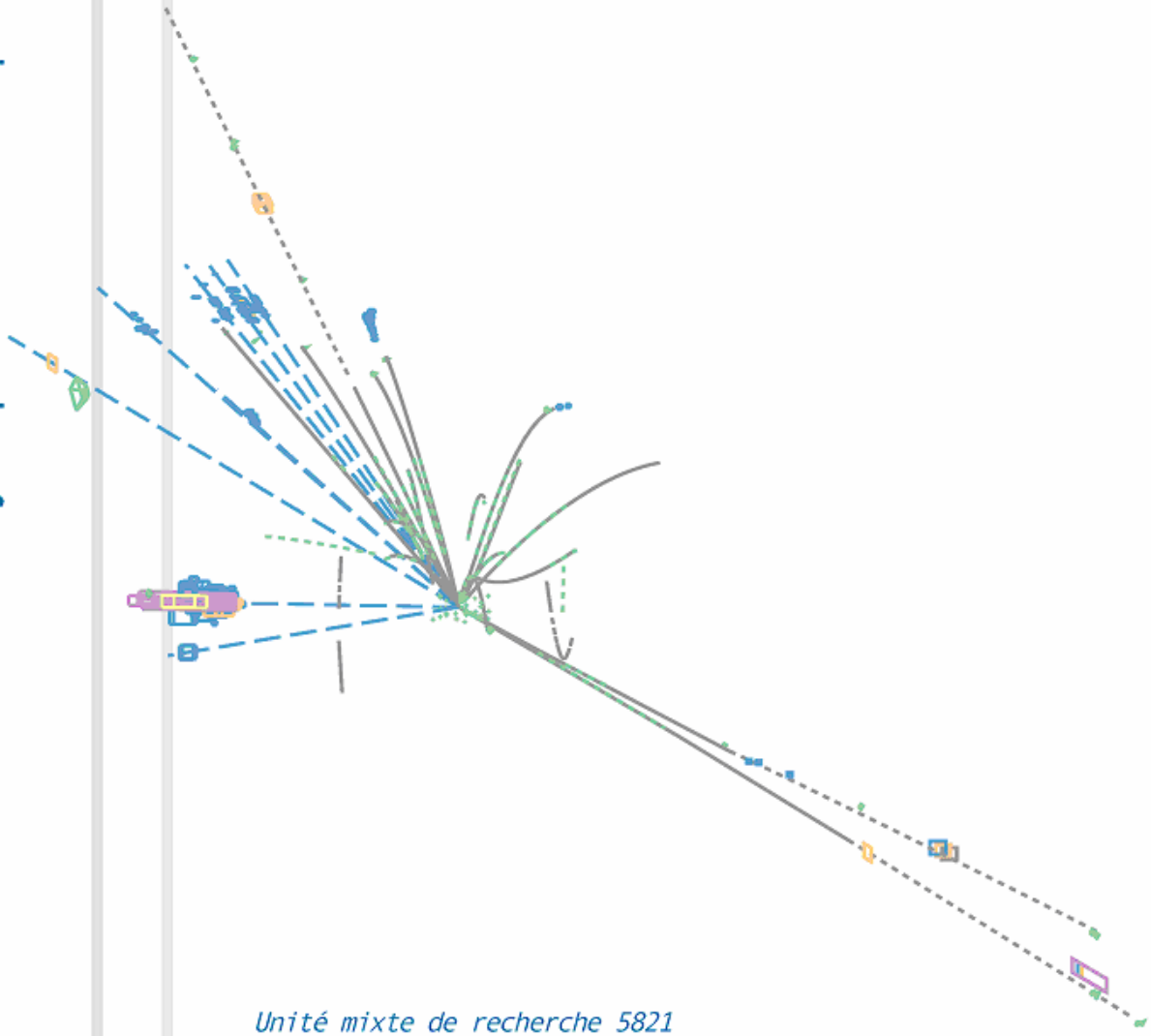

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1. Introduction

For the G0 experiment which take place in the Jefferson Laboratory, a whole of detection will be used for the determination of the contents in strange quarks of the nucleons by the measurement of the factors of weak form of the proton.
This experiment will have to measure low asymmetries (of about a 10^{-5}) in the elastic scattering of electrons polarized on the proton.
The experimental device is designed to detect the electrons diffused elastically on a target of liquid hydrogen. Those are emitted with angles of 110 degrees and are deviate by an electric field.
The system of detection consists of 8 octants placed around the beam axis, each one comprising 9 detectors placed near to the Cryostat (CED) and 14 detectors placed at approximately 2 meters of target (FPD).
The electrons resulting from elastic scattering are selected by certain coincidences CED(i) x FPD(j) due to the particular kinematics of the reaction

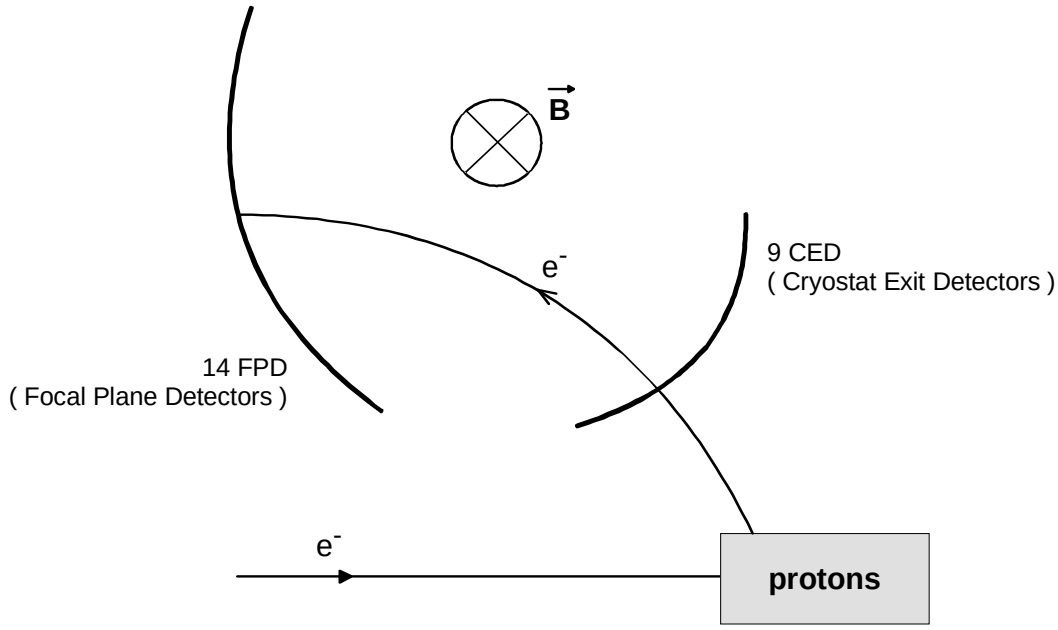


Figure 1 : diagram of the target and the detectors

The structure in time of the beam is broken up into sequences of 1/30s separated from 200µs, necessary for the reading of the physical data and the inversion of the HELICITY of the primary electrons (the HELICITY h corresponds to the direction of the electrons spin compared to its momentum).
The impulse sequence which will be sent on the target during the experiment is define below:

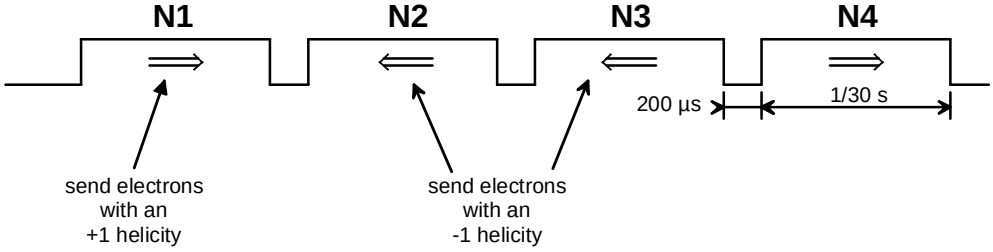


Figure 2 : Impulse sequence sent to the target

The measured asymmetry is then defined by:

$$A = \frac{N1 + N4 - N2 - N3}{N1 + N2 + N3 + N4}$$

Note: N1, N2, N3, N4 correspond to the number of coincidences for a given couple CED(i) X FPD(j).

During the period of 1/30s the beam is sent to a HF frequency (31,25 GHz) corresponding to a package of electrons all the 32 ns.
The events of elastic scattering are localized in a window in time (BPO) approximately 8 ns defined by a signal related to HF.

To realize the count of all the coincidences this board has developed.

2. Functionalities

This board is designed to manage 2 octants. Those being perfectly symmetrical, we define bellow only the functionality for one octant.

The functional diagram of the part active from the input to scalers is given in annex 1 (it is defined for one octant).
The coincidence are made inside two CPLD ALTERA and the count is done by 9 scalers components.
This scaler component[1] have 32 counters inside with a depth of 32 bits. It is an ASIC developed for the G0 experiment in AMS 0.6µ technology. It is also used in the G0 experiment VME scaler board SCALE32[2].
This component have, for each internal counter, a memory register which permit to count while the previous value of the counter is in it. This functionality permit for the acquisition to have more time for reading.

For one octant, one count is done for :

- Each input CED(i)[3] and FPD(i)[4] :
  The count is done an edge, this one being programmable.
  23 counters, called « **DIRECT_COUNTER** » are necessary to carry out this function

- Each rising edge on the inputs CED(i)[3] and FPD(j)[4] conditioned by a window of 8 ns given by the BPO detector (Beam Peak Off)
  23 counters, called « **NON_CONDITIONNED_DIRECT_COUNTER** », are necessary to carry out this function.

- Each coincidence between the signals CED(i)[3] and FPD(j)[4] and this in a window of 8 ns given by the BPO detector (Beam Pick off) and confirmed by an enabling signal called VALID (126 coincidences : 9 x 14).
  The signal VALID can be disabled by software.
  126 counters, called « **COINC_COUNTER** », are necessary to carry out this function.

- Each « **NON_CONDITIONNED_DIRECT_COUNTER** » input signal validate by an enabling signal called VALID.
  The signal VALID can be disabled by software, in this case the value of the CONDITIONNED DIRECT COUNTER is equal to the NON CONDITIONNED DIRECT COUNTER.
  23 counters, called « **CONDITIONNED_DIRECT_COUNTER** », are necessary to carry out this function.

- The multihits coincidences for each CED define by :

  $MC12\_(i)^3 = BPO \times VALID \times CED(i)^3 \times (\sum FPD(j)^4 = 2)$;

  $MC22\_(i)^3 = BPO \times VALID \times CED(i)^3 \times (\sum CED(i)^3 \geq 2) \times (\sum FPD(j)^4 \geq 2$
  $\text{or } \sum CED(i)^3 = 1) \times (\sum FPD(j)^4 \geq 3)$;

[1] COUNT32 : ASIC in CMOS technology included 32 scalers of 32 bits at 140 MHz

[2] SCALE 32 : 32 bit 32 counter board 140 MHz, IN VME FORMAT

[3] $0 \leq i \leq 8$

[4] $0 \leq j \leq 13$

The multihits coincidences for each FPD define by :

$MF12\_(j)^4 = BPO \times VALID \times FPD(j)^4 \times (\sum CED(i)^3 = 2)$;

$MF22\_(j)^4 = BPO \times VALID \times FPD(j)^4 \times (\sum FPD(j)^4 \geq 2) \times (\sum CED(i)^3 \geq 2$
Or $\sum FPD(j)^4 = 1) \times (\sum CED(i)^3 \geq 3)$;

46 counters respectively called « **MULTIHIT_12_COUNTER** » and « **MULTIHIT_22_COUNTER** » are necessary to carry out this function.

In the counter define before, there are 2 types of information :

- .. The counters which increment in the same BPO cycle (DIRECT_COUNTER , NON_CONDITIONNED_DIRECT_COUNTER)
- .. The counters which increment in the next BPO cycle (all the coincidences counters) due to an internal board timing which permit to make the coincidence between the different signal.

So for the 2 types of counter the memory command are different and the elementary counter can not be in the same SCALE32 component because the memory command is common for all the inside counter.
That is to say a total of 46 plus 195 counter per octant. The counter circuits used (COUNT32) have 32 counters, 9 components per octant are thus necessary to carry out all these countings.
The module managing 2 octants, it will be necessary to use 18 circuits.

The reading of all counter will be made through the VXI bus.

2.1. Acquiring the value for one pulse

As shows the below figure, the input and the coincidence counter are incremented when the MPS signal is active.
When it goes inactive an internal board logic inhibit the input counter, memorize into the on chip memories the value of the counter and then reset them for a new acquisition cycle.
The acquisition system have the one time pulse for reading all the memorized counter value.

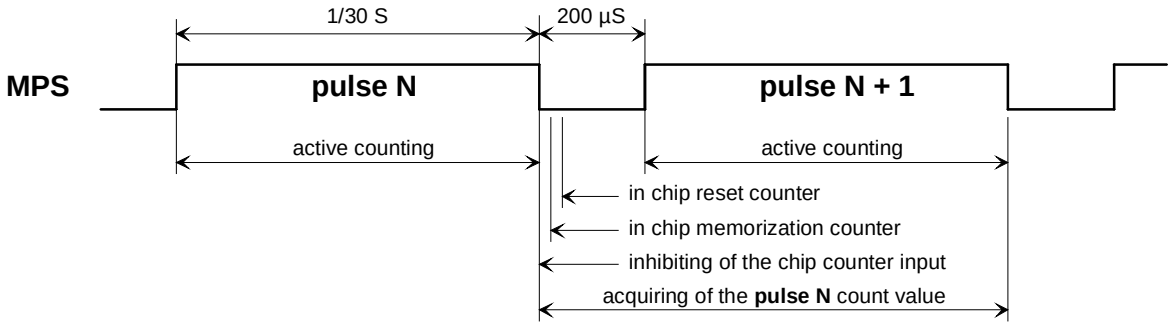


Figure 3 : Counter value acquiring sequence

2.2. Relative position of the signals

The figure below shows the relative position of the signals in the pulse.
A detailed diagram, with timing, is done in annex 3.

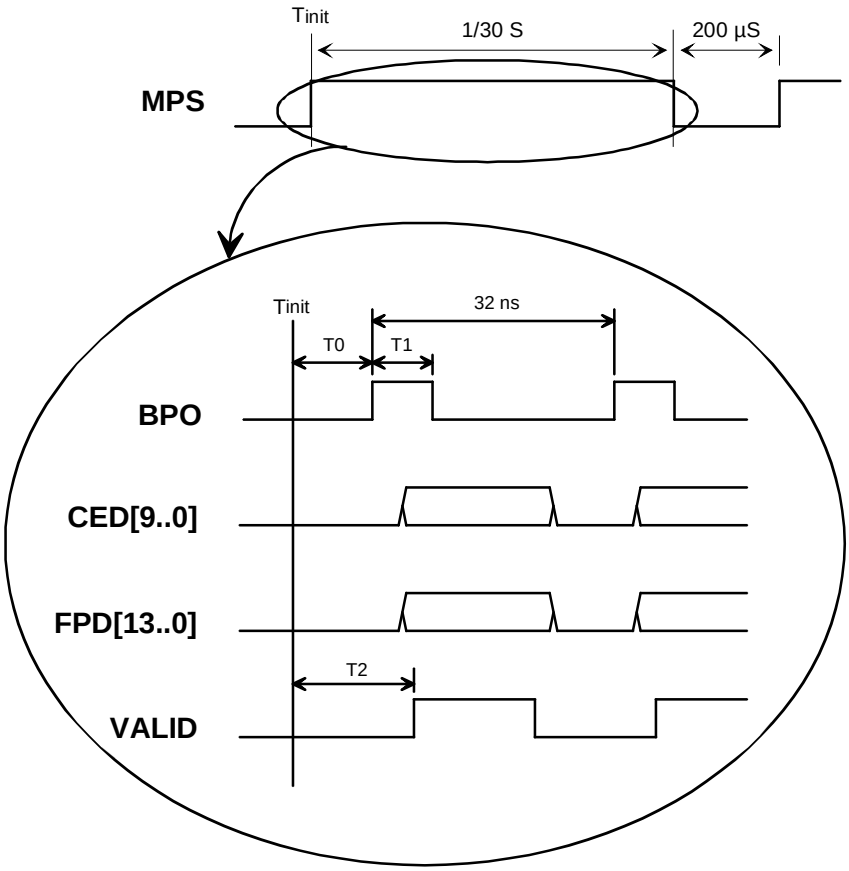


Figure 4 : Acquiring sequence diagram

2.3. Coincidences output (SCOINCA, SCOINCB)

Some specific coincidences must be output for look up or count them. This coincidences are characteristic for a type of experiment. The following paragraph shows them (physics simulation paragraph) .
The board can output one or some of the available coincidences for a type of experiment. The available coincidences is determined by a FPGA specific programming files in conjunction with the type of experiment. The configuration is made for the 2 octants
The choice, of which coincidences is output, is done by writing 48 bits into an internal onboard register (DCOINC register). Each bit represents one coincidence, an 1 validate it and a 0 inhibit it.
The definition of this register is different for each type of experiment and it is explain in the following paragraph (synthesis paragraph).
For writing the 48 validation bits into the 16 bit register DCOINC the user must write three 16 bit word in a specific order.

2.3.1. Physics simulation

Represents a coincidence which must be available and can be selected
Represents a coincidence which can be available and can be selected

2.3.1.1. LH2 (all overcome energy)

		FPD															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CED	0																
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																

2.3.1.2. LD2 (all overcome energy)

		FPD															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CED	0																
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																

2.3.1.3. LH2 + LD2 (all overcome energy)

		FPD															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CED	0																
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																

2.3.2. Synthesis

2.3.2.1. FPGA programming file “INPUTDA”

		FPD													
		0	1	2	3	4	5	6	7	8	9	10	11	12	13
CED	0														
	1														
	2														
	3														
	4														
	5														
	6														
	7														
	8														

Writing sequence :

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st	0	0	0	0	0	0	C8F13	C8F12	C7F12	C7F11	C7F10	C6F12	C6F11	C6F10	C6F9	C5F11
2nd	C5F10	C5F9	C5F8	C5F7	C4F10	C4F9	C4F8	C4F7	C4F6	C3F9	C3F8	C3F7	C3F6	C3F5	C2F8	C2F7
3rd	C2F6	C2F5	C2F4	C1F8	C1F7	C1F6	C1F5	C1F4	C1F3	C8F8	C0F7	C0F6	C0F5	C0F4	C0F3	C0F2

CxFy represents the coincidence CEDxFPDy

2.3.2.2. FPGA programming file "INPUTDB"

		FPD													
		0	1	2	3	4	5	6	7	8	9	10	11	12	13
CED	0														
	1														
	2														
	3														
	4														
	5														
	6														
	7														
	8														

Writing sequence :

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st	0	0	0	0	C8F13	C8F12	C8F11	C7F12	C7F11	C7F10	C7F9	C6F11	C6F10	C6F9	C6F8	C5F10
2nd	C5F9	C5F8	C5F7	C5F6	C4F9	C4F8	C4F7	C4F6	C4F5	C3F8	C3F7	C3F6	C3F5	C3F4	C2F7	C2F6
3rd	C2F5	C2F4	C2F3	C1F7	C1F6	C1F5	C1F4	C1F3	C1F2	C0F7	C0F6	C0F5	C0F4	C0F3	C0F2	C0F1

CxFy represents the coincidence CEDxFPDy

2.3.2.3. FPGA programming file " INPUTDC "

		FPD													
		0	1	2	3	4	5	6	7	8	9	10	11	12	13
CED	0														
	1														
	2														
	3														
	4														
	5														
	6														
	7														
	8														

Writing sequence :

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st	0	0	0	C8F13	C8F12	C8F11	C8F10	C7F11	C7F10	C7F9	C7F8	C6F10	C6F9	C6F8	C6F7	C5F9
2nd	C5F8	C5F7	C5F6	C5F5	C4F8	C4F7	C4F6	C4F5	C4F4	C3F7	C3F6	C3F5	C3F4	C3F3	C2F6	C2F5
3rd	C2F4	C2F3	C2F2	C1F6	C1F5	C1F4	C1F3	C1F2	C1F1	C0F6	C0F5	C0F4	C0F3	C0F2	C0F1	C0F0

CxFy represents the coincidence CEDxFPDy

2.4. Board position in the data acquisition system

The Annex 25 : Board position shows the relative position of the board in Data acquisition System.

3. Front Panel

The board has on his front end several connectors which permit to do the connection between this board and the others.
There is 2 types of connectors :

- connectors for flat cable (4 x HE10-34) : for connecting the CED/FPD signals of the 2 octants
- coaxial connector (14 x LEMO type) :
  - 5 of them are for the input control
  - 8 of them are for the output control (viewer of internal board signal)
  - 1 is unaffected.

3.1. CED/FPD input signals

The ced/fpd input signal are in differential ECL technology and the pinout is given in Annex 4 : .

3.2. Input control

The 5 input control signals are in NIM level and manage 3 functions :

- Beam Pick Off function (BPO_in input)
- Valid function (VALID input)
- Counter value memorization (Inhibit, LO and RST input)

BPO_in : This is the validation input (GATE) for the CED/FPD signals.
This signal has a active width of 8 ns for a 32 ns period (duty cycle 25 %)

VALID : This is the validation input for the coincidences.
A rising front into the current cycle (32 ns cycle) validate the coincidence CED/FPD.
This input can be disable by a software command into the command register of the board and all the coincidences are validate. By default this input is active.

The 3 control signal below are about the counter value memorization command. This signal is describe in sequence.

INHIBIT : This input inhibit the on board counter input (COUNT32)[5] which count the input and the coincidences.
This input can be disable or disable by a software command into the command register of the board. This command disable or enable the RST input and the LO input too. If this input is disable an internal mechanism manage the memorization command in conjunction with a back plane signal (MPS).
By default this input is inactive.

LO : This input memorize, on the low to up changed state, the counter values into intermediary registers inside the onboard counter component (COUNT32)[5] which count the input and the coincidences.
This input can be disable or disable by a software command into the command register of the board. This command disable or enable the INHIBIT input and the RST input too. If this input is disable an internal mechanism manage the memorization command in conjunction with a back plane signal (MPS).
By default this input is inactive.

RST : This input reset the internal contents of the on board counter (COUNT32)[5] which count the input and the coincidences.
This input can be disable or disable by a software command into the command register of the board. This command disable or enable the INHIBIT input and the LO input too. If this input is disable an internal mechanism manage the memorization command in conjunction with a back plane signal (MPS).
By default this input is inactive.

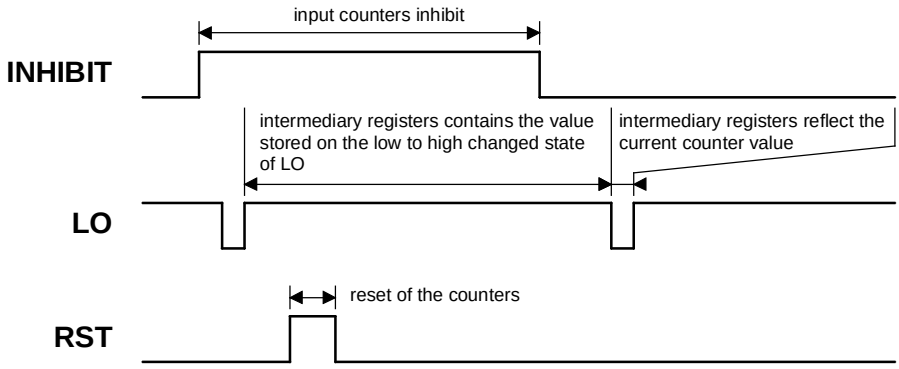


Figure 5 : command counter sequencing

3.3. Output control

This 8 output serve for the control of the internal functionality.
Some of them are common to the 2 octants (BPOout, SVALID).
The control signals are in NIM level

SCEDA, SFPDA,
SCEDB, SFPDB : these outputs are the logical OR of some internal signals relative to the CED and FPD signals. These internal signals are defined by an internal board register describe below (ETAT register)

[5] COUNT32 : ASIC in CMOS technology included 32 scalers of 32 bits at 140 MHz

SCOINCA, SCOINCB these outputs are for the specific coincidences (see the explain in the paragraph 2.3 Coincidences output (SCOINCA, SCOINCB)).

BPOout this output shown the different command signal in the acquisition sequence (Clock and reset signal of the flip flop in the different stage).
The command signal shown is defined by an internal board register describe below (ETAT register)

SVALID this signal is the output of the VALID first stage acquisition (see the front end diagram)

4. Board addressing method, Internal register and address decoder :

The memory map is defined like below :

- Counter for the first octant :
  - Counter space : @base
  - Command register space : @base + 400h
- Counter for the second octant :
  - Counter space : @base + 800h
  - Command register space : @base + C00h
- Counter for the two octant
  - Counter space : @base + 1000h
  - Command register space : @base + 1400h
- Internal register
  - COINC register : @base + 1800h
  - ETAT register : @base + 1804h
  - IT register : @base + 1880h
  - CHOIX register : @base + 1884h
- MPS delay : @base + 1900h

4.1. Board addressing (determination of @base)

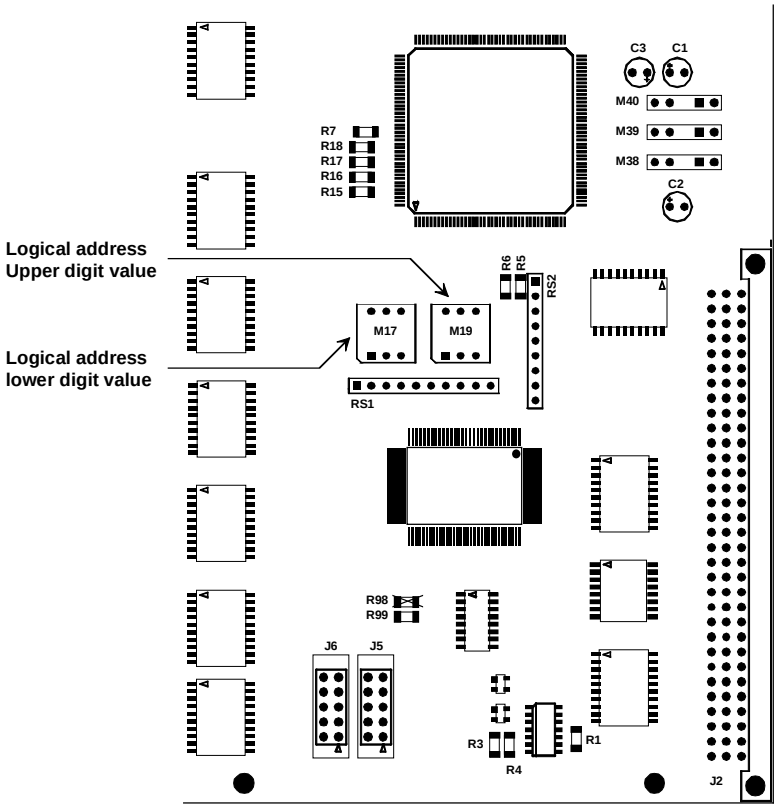
To manage the VXI interface, the board used a dedicated integrate circuit (IT9010) designed by Interface Technology.
This integrated circuit manage all the VXI accesses with a minimum of external circuit, the users have only to indicate the board logical address to permit the accesses to configure this one, especially the board base address in the A32/D32 space.
The board address, for the configuration, can be done like the following formula :

Address_board_configuration = 0x”C000” + (logical_address x 0x”40”)

To have more information’s about the VXI controller internal register see the IT9010 users manual presents on the Interface Technology web site (www.interfacetech.com)

4.1.1. Board logical address assignment

The board logical address is assigned by two rotary switches located on the printed board (near the VXI connector).
The value goes 0 to 0x”FF” (hexadecimal value) where 0x”FF” is used for a dynamic board address, so the logical address is assigned by the computer .



4.2. Internal register

4.2.1. DCOINC register

It is a 16 bit register which serves to select which specific coincidences or which ored specific coincidences is present on the SCOINCA and SCOINCB output.
The user must write three 16 bit word for initializing completely this function. An one in a bit validate the coincidence , a 0 inhibit it.
The definition of this register depend of the FPGA file programming (INPUTDA file by default)

4.2.1.1. FPGA programming file "INPUTDA"

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st	0	0	0	0	0	0	C8F13	C8F12	C7F12	C7F11	C7F10	C6F12	C6F11	C6F10	C6F9	C5F11
2nd	C5F10	C5F9	C5F8	C5F7	C4F10	C4F9	C4F8	C4F7	C4F6	C3F9	C3F8	C3F7	C3F6	C3F5	C2F8	C2F7
3rd	C2F6	C2F5	C2F4	C1F8	C1F7	C1F6	C1F5	C1F4	C1F3	C8F8	C0F7	C0F6	C0F5	C0F4	C0F3	C0F2

4.2.1.2. FPGA programming file "INPUTDB"

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st	0	0	0	0	C8F13	C8F12	C8F11	C7F12	C7F11	C7F10	C7F9	C6F11	C6F10	C6F9	C6F8	C5F10
2nd	C5F9	C5F8	C5F7	C5F6	C4F9	C4F8	C4F7	C4F6	C4F5	C3F8	C3F7	C3F6	C3F5	C3F4	C2F7	C2F6
3rd	C2F5	C2F4	C2F3	C1F7	C1F6	C1F5	C1F4	C1F3	C1F2	C0F7	C0F6	C0F5	C0F4	C0F3	C0F2	C0F1

4.2.1.3. FPGA programming file "INPUTDC"

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st	0	0	0	C8F13	C8F12	C8F11	C8F10	C7F11	C7F10	C7F9	C7F8	C6F10	C6F9	C6F8	C6F7	C5F9
2nd	C5F8	C5F7	C5F6	C5F5	C4F8	C4F7	C4F6	C4F5	C4F4	C3F7	C3F6	C3F5	C3F4	C3F3	C2F6	C2F5
3rd	C2F4	C2F3	C2F2	C1F6	C1F5	C1F4	C1F3	C1F2	C1F1	C0F6	C0F5	C0F4	C0F3	C0F2	C0F1	C0F0

4.2.2. ETAT register

It is a 16 bit register which define the functional mode of the board.
This register is cleared a the power up of the board.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W			ETAT[13]	ETAT[12]	ETAT[11]	VAL_COM	ETAT[9]	ETAT[8]	ETAT[7]	ETAT[6]	ETAT[5]	ETAT[4]	ETAT[3]	ETAT[2]	ETAT[1]	ETAT[0]
R	0	0	ETAT[13]	ETAT[12]	ETAT[11]	V_COM	ETAT[9]	ETAT[8]	ETAT[7]	ETAT[6]	ETAT[5]	ETAT[4]	ETAT[3]	ETAT[2]	ETAT[1]	ETAT[0]

The bits are defined like below :

ETAT[13] : input PATTERN of the counter components (COUNT32 ASIC component)
A rising edge on this bit memorize the input state of all the individual counter. The result is read in the PATTERN register of the counter component (see the COUNT32 data sheet)

ETAT[12] : input POLAR of the counter components (COUNT32 ASIC component).
This bit is a global command signal for all the counter and determine which input edge is counted. This bit is used in conjunction with the POLAR register of the counter component (see the COUNT32 data sheet)

0 : rising edge
1 : falling edge

ETAT[11] : input TEST of the counter components (COUNT32 ASIC component)
This bit serves for the test and when it is set to one, the 32 bit individual counter are putted in four 8 bit counter with a common input. This configuration permit to count the maximum value in a minimum time. (see the COUNT32 data sheet)

VALCOM : it is a write only bit and serves for the test.
When an 1 is writing in this bit, an internal mechanism generate 170 pulses on the COMMUN input of the counter components. Each individual counter must increment his internal value with the number of clocks generated.

V_COM : it is a read on bit and it is used in conjunction with the VALCOM bit for the test.
When this bit is high the pulses generation is in progress.

ETAT[9..8] : define which signal are applying on the INHIBC and INHIBNC input signal of the COUNT32 ASIC component.

ETAT[9]	ETAT[8]	INHIBC	INHIBNC
0	0	MPSD	MPS
0	1	MPS	MPS
1	0	MPS1	MPS1
1	1	MPSD	MSPD

- **MPS signal** is the backboard Macro Pulse Synchronization signal present on the VXI connector. It is delivered by the Interface Box module.
- **MPSD signal** is the delayed Macro Pulse Synchronization signal. The value of the delay is defined in the onboard DELAY register. The delay is made on the CEDFPD board.

- **MPS1 signal** is the backboard Macro Pulse Synchronization signal sampled by the SYSCLOCK clock (16 MHz). The sample is made on the CEDFPD board.
  The time information for the MPS1 signal is :
  MPS1 = MPS + 1 CK16 + ΔCK16

ETAT[7] : define which signals are applying on the control signals of the COUNT32 ASIC component.
The control signals of the COUNT32 ASIC component define :
- the time when the coincidence are counted
- the time when the COUNT32 ASIC counter value are put in the intermediary register to be read
- the time when the COUNT32 ASIC counter are cleared

when this bit is set to :
- 0 it is the onboard state machine which managed these signals
- 1 it is the external signal present on the LO, INHIBIT and RST input board which managed the control signals of the COUNT32 ASIC component.

ETAT6 : when is set to 1 the input flip flop (Flip Flop open when the BPO is active) are put in a cleared state (no coincidence can be counted)

ETAT[5..3] : define the signal present on the BPOout output board.

ETAT5	ETAT4	ETAT3	BPOout
0	0	0	BPO in
0	0	1	VVALID
0	1	0	BPO2
0	1	1	BPO1
1	0	0	RESET0
1	0	1	RVALID
1	1	0	INSPEC
1	1	1	0

BPO in input board BPO signal
VVALID sample signal for the input board VALID signal
BPO2 validation signal for the coincidences
BPO1 validation signal for the intermediary memorization of the coincidence : BPO and the input signal CED, FPD
RESET0 reset signal for the CEDx, FPDx signal input flip flop (validate flip flop when the BPO signal is active)
RVALID reset signal for the VALID signal input flip flop
INSPEC signal issue of the FPGA component

ETAT[2..1] : define the signal present on the SCED (A and B) and the SFPD (A and B) output board.

ETAT2	ETAT1	SCED	SFPD
0	0	CCED	CFPD
0	1	DCED	DFPD
1	0	CCED	DCED
1	1	CFPD	DFPD

CCED, CFPD : signals of the input CED,FPD after the input flip flop (validate FLIP FLOP when the BPO signal is active)

DCED, DFPD : signals CCED and CFPD sampled by the BPO1 signal

ETAT0 : State of the input VALID in the final coincidence

When set to 0, the coincidence counted is function of the VALID input.
The equation is then :
COINC(CEDx,FPDx) while BPO signal is valid and VALID signal active

When set to 1, the coincidence counted is not function of the VALID input.
The equation is then :
COINC(CEDx,FPDx) while BPO signal is valid

4.2.3. IT Register

The board can generate an interrupt on the VXI bus when it detect a rising edge on the MPS signal.
The user must :

- validate this option (by default this option is not validated)
- indicate which interrupt level must be generated

When an interrupt is generated by the CEDFPD board, the interrupt vector generated at the VXI interrupt acknowledge cycle is equal to the board VXI logical address designed by the value of the rotary switch present on the board;
If POWERPC or 68000 processor family computer unit is used, the interrupt software is going at an address equal to the value of the logical address multiplied by 4 (Annex 24 : Interrupt vector address jump shows the address where the interrupt program must be located, if POWERPC or 68000 processor family computer unit is used, function of the board logical address).
At the VXI interrupt acknowledge cycle the user must invalidated the interrupt board and then revalidate it to allow a new interrupt.
The interrupt validate and the interrupt level is defined in the IT register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W										INT3	INT2	INT1			V_IRQ	
R	0	0	0	0	0	0	0	0	0	INT3	INT2	INT1	0	0	V_IRQ	IT

V_IRQ : Interrupt validation bit

0 : no interrupt is generated by the board
1 : an interrupt is generated by the board on a rising edge of the MPS signal

INT[3..1] : define which VXI interrupt line is driven when an interrupt occur (when a value 0 is written in this bit no interrupt is generated by the board)

IT : this bit is read only and define the state of the interrupt

0 : no interrupt is generated
1 : interrupt is generated

Note : if this option is used and if POWERPC or 68000 processor family computer unit is used, the board logical address must not be less than 0x"40" to not used an interrupt vector assigned to an internal event processor.

4.2.4. CHOIX register

The CHOIX register is for the future functionality.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W															CHOIX1	CHOIX0
R	0	0	0	0	0	0	0	0	0	0	0	0	0	VCOINC	CHOIX1	CHOIX0

It is define like this :

CHOIX[1..0] : liaison bit with the EPLD CEDFPD (actually not in use)

VCOINC : busy indicator which indicate the state of the serial line which load the coincidence number line to be saw on the SCOINC output.
It is used in coincidence with the DCOINC register.

0 : line is ready
1 : line is busy

4.2.5. DELAY register

This register is a write on register and define the delay between the MPS signal and the MPSD signal.
Due to the internal delay of the component there is a minimum delay which is equal to 12,5 ns.
The maximum delay is equal to 150 ns.
The delay is define like below :

DELAY = 12,5 ns + (Delay register value) x (137,5 / 255)

4.3. Counter Space

The space « counters » and « command/state register » for each octant, are distinct to have a continuous space for the 2 types of function : counter and characterization.

4.3.1. Circuit 0 (@base)

Address	Counter	Name	Type
@base	0	*Non available*	
@base + 0004	1	*Non available*	
@base + 0008	2	*Non available*	
@base + 000C	3	*Non available*	
@base + 0010	4	*Non available*	
@base + 0014	5	*Non available*	
@base + 0018	6	A_CCED0	CED0 Non Conditioned Direct Counter
@base + 001C	7	A_CCED1	CED1 Non Conditioned Direct Counter
@base + 0020	8	A_CCED2	CED2 Non Conditioned Direct Counter
@base + 0024	9	A_CCED3	CED3 Non Conditioned Direct Counter
@base + 0028	10	A_CCED4	CED4 Non Conditioned Direct Counter
@base + 002C	11	A_CCED5	CED5 Non Conditioned Direct Counter
@base + 0030	12	A_CCED6	CED6 Non Conditioned Direct Counter
@base + 0034	13	A_CCED7	CED7 Non Conditioned Direct Counter
@base + 0038	14	A_CCED8	CED8 Non Conditioned Direct Counter
@base + 003C	15	A_CFPD0	FPD0 Non Conditioned Direct Counter
@base + 0040	16	A_CFPD1	FPD1 Non Conditioned Direct Counter
@base + 0044	17	A_CFPD2	FPD2 Non Conditioned Direct Counter
@base + 0048	18	A_CFPD3	FPD3 Non Conditioned Direct Counter
@base + 004C	19	A_CFPD4	FPD4 Non Conditioned Direct Counter
@base + 0050	20	A_CFPD5	FPD5 Non Conditioned Direct Counter
@base + 0054	21	A_CFPD6	FPD6 Non Conditioned Direct Counter
@base + 0058	22	A_CFPD7	FPD7 Non Conditioned Direct Counter
@base + 005C	23	A_CFPD8	FPD8 Non Conditioned Direct Counter
@base + 0060	24	A_CFPD9	FPD9 Non Conditioned Direct Counter
@base + 0064	25	A_CFPD10	FPD10 Non Conditioned Direct Counter
@base + 0068	26	A_CFPD11	FPD11 Non Conditioned Direct Counter
@base + 006C	27	A_CFPD12	FPD12 Non Conditioned Direct Counter
@base + 0070	28	A_CFPD13	FPD13 Non Conditioned Direct Counter
@base + 0074	29	*Non available*	
@base + 0078	30	*Non available*	
@base + 007C	31	*Non available*	

4.3.2. Circuit 1 (@base + 0080)

Address	Counter	Name	Type
@base + 0080	0	A_CC3	CED3 Conditioned Direct Counter
@base + 0084	1	A_CC4	CED4 Conditioned Direct Counter
@base + 0088	2	A_CC5	CED5 Conditioned Direct Counter
@base + 008C	3	A_CC6	CED6 Conditioned Direct Counter
@base + 0090	4	A_CC7	CED7 Conditioned Direct Counter
@base + 0094	5	A_CC8	CED8 Conditioned Direct Counter
@base + 0098	6	A_CF0	FPD0 Conditioned Direct Counter
@base + 009C	7	A_CF1	FPD1 Conditioned Direct Counter
@base + 00A0	8	A_CF2	FPD2 Conditioned Direct Counter
@base + 00A4	9	A_CF3	FPD3 Conditioned Direct Counter
@base + 00A8	10	A_CF4	FPD4 Conditioned Direct Counter
@base + 00AC	11	A_CF5	FPD5 Conditioned Direct Counter
@base + 00B0	12	A_CF6	FPD6 Conditioned Direct Counter
@base + 00B4	13	A_CF7	FPD7 Conditioned Direct Counter
@base + 00B8	14	A_CF8	FPD8 Conditioned Direct Counter
@base + 00BC	15	A_CF9	FPD9 Conditioned Direct Counter
@base + 00C0	16	A_CF10	FPD10 Conditioned Direct Counter
@base + 00C4	17	A_CF11	FPD11 Conditioned Direct Counter
@base + 00C8	18	A_CF12	FPD12 Conditioned Direct Counter
@base + 00CC	19	A_CF13	FPD13 Conditioned Direct Counter
@base + 00D0	20	A_M12_C0	CED0 Multihit_12_counter (CED0 and 2 FPD)
@base + 00D4	21	A_M12_C1	CED1 Multihit_12_counter (CED1 and 2 FPD)
@base + 00D8	22	A_M12_C2	CED2 Multihit_12_counter (CED2 and 2 FPD)
@base + 00DC	23	A_M12_C3	CED3 Multihit_12_counter (CED3 and 2 FPD)
@base + 00E0	24	A_M12_C4	CED4 Multihit_12_counter (CED4 and 2 FPD)
@base + 00E4	25	A_M12_C5	CED5 Multihit_12_counter (CED5 and 2 FPD)
@base + 00E8	26	A_M12_C6	CED6 Multihit_12_counter (CED6 and 2 FPD)
@base + 00EC	27	A_M12_C7	CED7 Multihit_12_counter (CED7 and 2 FPD)
@base + 00F0	28	A_M12_C8	CED8 Multihit_12_counter (CED8 and 2 FPD)
@base + 00F4	29	A_M12_F0	FPD0 Multihit_12_counter (PFD0 and 2 CED)
@base + 00F8	30	A_M12_F1	FPD1 Multihit_12_counter (PFD1 and 2 CED)
@base + 00FC	31	A_M12_F2	FPD2 Multihit_12_counter (PFD2 and 2 CED)

4.3.3. Circuit 2 (@base + 0100)

Address	Counter	Name	Type
@base + 0100	0	A_M12_F3	FPD3 Multihit_12_counter (PFD3 and 2 CED)
@base + 0104	1	A_M12_F4	FPD4 Multihit_12_counter (PFD4 and 2 CED)
@base + 0108	2	A_M12_F5	FPD5 Multihit_12_counter (PFD5 and 2 CED)
@base + 010C	3	A_M12_F6	FPD6 Multihit_12_counter (PFD6 and 2 CED)
@base + 0110	4	A_M12_F7	FPD7 Multihit_12_counter (PFD7 and 2 CED)
@base + 0114	5	A_M12_F8	FPD8 Multihit_12_counter (PFD8 and 2 CED)
@base + 0118	6	A_M12_F9	FPD9 Multihit_12_counter (PFD9 and 2 CED)
@base + 011C	7	A_M12_F10	FPD10 Multihit_12_counter (PFD10 and 2 CED)
@base + 0120	8	A_M12_F11	FPD11 Multihit_12_counter (PFD11 and 2 CED)
@base + 0124	9	A_M12_F12	FPD12 Multihit_12_counter (PFD12 and 2 CED)
@base + 0128	10	A_M12_F13	FPD13 Multihit_12_counter (PFD13 and 2 CED)
@base + 012C	11	A_M22_C0	CED0 Multihit_22_counter (CED0 and MULTI ≥ 3)
@base + 0130	12	A_M22_C1	CED1 Multihit_22_counter (CED1 and MULTI ≥ 3)
@base + 0134	13	A_M22_C2	CED2 Multihit_22_counter (CED2 and MULTI ≥ 3)
@base + 0138	14	A_M22_C3	CED3 Multihit_22_counter (CED3 and MULTI ≥ 3)
@base + 013C	15	A_M22_C4	CED4 Multihit_22_counter (CED4 and MULTI ≥ 3)
@base + 0140	16	A_M22_C5	CED5 Multihit_22_counter (CED5 and MULTI ≥ 3)
@base + 0144	17	A_M22_C6	CED6 Multihit_22_counter (CED6 and MULTI ≥ 3)
@base + 0148	18	A_M22_C7	CED7 Multihit_22_counter (CED7 and MULTI ≥ 3)
@base + 014C	19	A_M22_C8	CED8 Multihit_22_counter (CED8 and MULTI ≥ 3)
@base + 0150	20	A_M22_F0	FPD0 Multihit_22_counter (FPD0 and MULTI ≥ 3)
@base + 0154	21	A_M22_F1	FPD1 Multihit_22_counter (FPD1 and MULTI ≥ 3)
@base + 0158	22	A_M22_F2	FPD2 Multihit_22_counter (FPD2 and MULTI ≥ 3)
@base + 015C	23	A_M22_F3	FPD3 Multihit_22_counter (FPD3 and MULTI ≥ 3)
@base + 0160	24	A_M22_F4	FPD4 Multihit_22_counter (FPD4 and MULTI ≥ 3)
@base + 0164	25	A_M22_F5	FPD5 Multihit_22_counter (FPD5 and MULTI ≥ 3)
@base + 0168	26	A_M22_F6	FPD6 Multihit_22_counter (FPD6 and MULTI ≥ 3)
@base + 016C	27	A_M22_F7	FPD7 Multihit_22_counter (FPD7 and MULTI ≥ 3)
@base + 0170	28	A_M22_F8	FPD8 Multihit_22_counter (FPD8 and MULTI ≥ 3)
@base + 0174	29	A_M22_F9	FPD9 Multihit_22_counter (FPD9 and MULTI ≥ 3)
@base + 0178	30	A_M22_F10	FPD10 Multihit_22_counter (FPD10 and MULTI ≥ 3)
@base + 017C	31	A_M22_F11	FPD11 Multihit_22_counter (FPD11 and MULTI ≥ 3)

4.3.4. Circuit 3 (@base + 0180)

Address	Counter	Name	Type
@base + 0180	0	A_M22_F12	FPD12 Multihit_22_counter (FPD12 and MULTI ≥ 3)
@base + 0184	1	A_M22_F13	FPD13 Multihit_22_counter (FPD13 and MULTI ≥ 3)
@base + 0188	2	A_COINC_0_0	CED0_FPD0_coincidence_counter
@base + 018C	3	A_COINC_0_1	CED0_FPD1_coincidence_counter
@base + 0190	4	A_COINC_0_2	CED0_FPD2_coincidence_counter
@base + 0194	5	A_COINC_0_3	CED0_FPD3_coincidence_counter
@base + 0198	6	A_COINC_0_4	CED0_FPD4_coincidence_counter
@base + 019C	7	A_COINC_0_5	CED0_FPD5_coincidence_counter
@base + 01A0	8	A_COINC_0_6	CED0_FPD6_coincidence_counter
@base + 01A4	9	A_COINC_0_7	CED0_FPD7_coincidence_counter
@base + 01A8	10	A_COINC_0_8	CED0_FPD8_coincidence_counter
@base + 01AC	11	A_COINC_0_9	CED0_FPD9_coincidence_counter
@base + 01B0	12	A_COINC_0_10	CED0_FPD10_coincidence_counter
@base + 01B4	13	A_COINC_0_11	CED0_FPD11_coincidence_counter
@base + 01B8	14	A_COINC_0_12	CED0_FPD12_coincidence_counter
@base + 01BC	15	A_COINC_0_13	CED0_FPD13_coincidence_counter
@base + 01C0	16	A_COINC_1_0	CED1_FPD0_coincidence_counter
@base + 01C4	17	A_COINC_1_1	CED1_FPD1_coincidence_counter
@base + 01C8	18	A_COINC_1_2	CED1_FPD2_coincidence_counter
@base + 01CC	19	A_COINC_1_3	CED1_FPD3_coincidence_counter
@base + 01D0	20	A_COINC_1_4	CED1_FPD4_coincidence_counter
@base + 01D4	21	A_COINC_1_5	CED1_FPD5_coincidence_counter
@base + 01D8	22	A_COINC_1_6	CED1_FPD6_coincidence_counter
@base + 01DC	23	A_COINC_1_7	CED1_FPD7_coincidence_counter
@base + 01E0	24	A_COINC_1_8	CED1_FPD8_coincidence_counter
@base + 01E4	25	A_COINC_1_9	CED1_FPD9_coincidence_counter
@base + 01E8	26	A_COINC_1_10	CED1_FPD10_coincidence_counter
@base + 01EC	27	A_COINC_1_11	CED1_FPD11_coincidence_counter
@base + 01F0	28	A_COINC_1_12	CED1_FPD12_coincidence_counter
@base + 01F4	29	A_COINC_1_13	CED1_FPD13_coincidence_counter
@base + 01F8	30	A_COINC_2_0	CED2_FPD0_coincidence_counter
@base + 01FC	31	A_COINC_2_1	CED2_FPD1_coincidence_counter

4.3.5. Circuit 4 (@base + 0200)

Address	Counter	Name	Type
@base + 0200	0	A_COINC_2_2	CED2_FPD2_coincidence_counter
@base + 0204	1	A_COINC_2_3	CED2_FPD3_coincidence_counter
@base + 0208	2	A_COINC_2_4	CED2_FPD4_coincidence_counter
@base + 020C	3	A_COINC_2_5	CED2_FPD5_coincidence_counter
@base + 0210	4	A_COINC_2_6	CED2_FPD6_coincidence_counter
@base + 0214	5	A_COINC_2_7	CED2_FPD7_coincidence_counter
@base + 0218	6	A_COINC_2_8	CED2_FPD8_coincidence_counter
@base + 021C	7	A_COINC_2_9	CED2_FPD9_coincidence_counter
@base + 0220	8	A_COINC_2_10	CED2_FPD10_coincidence_counter
@base + 0224	9	A_COINC_2_11	CED2_FPD11_coincidence_counter
@base + 0228	10	A_COINC_2_12	CED2_FPD12_coincidence_counter
@base + 022C	11	A_COINC_2_13	CED2_FPD13_coincidence_counter
@base + 0230	12	A_COINC_3_0	CED3_FPD0_coincidence_counter
@base + 0234	13	A_COINC_3_1	CED3_FPD1_coincidence_counter
@base + 0238	14	A_COINC_3_2	CED3_FPD2_coincidence_counter
@base + 023C	15	A_COINC_3_3	CED3_FPD3_coincidence_counter
@base + 0240	16	A_COINC_3_4	CED3_FPD4_coincidence_counter
@base + 0244	17	A_COINC_3_5	CED3_FPD5_coincidence_counter
@base + 0248	18	A_COINC_3_6	CED3_FPD6_coincidence_counter
@base + 024C	19	A_COINC_3_7	CED3_FPD7_coincidence_counter
@base + 0250	20	A_COINC_3_8	CED3_FPD8_coincidence_counter
@base + 0254	21	A_COINC_3_9	CED3_FPD9_coincidence_counter
@base + 0258	22	A_COINC_3_10	CED3_FPD10_coincidence_counter
@base + 025C	23	A_COINC_3_11	CED3_FPD11_coincidence_counter
@base + 0260	24	A_COINC_3_12	CED3_FPD12_coincidence_counter
@base + 0264	25	A_COINC_3_13	CED3_FPD13_coincidence_counter
@base + 0268	26	A_COINC_4_0	CED4_FPD0_coincidence_counter
@base + 026C	27	A_COINC_4_1	CED4_FPD1_coincidence_counter
@base + 0270	28	A_COINC_4_2	CED4_FPD2_coincidence_counter
@base + 0274	29	A_COINC_4_3	CED4_FPD3_coincidence_counter
@base + 0278	30	A_COINC_4_4	CED4_FPD4_coincidence_counter
@base + 027C	31	A_COINC_4_5	CED4_FPD5_coincidence_counter

4.3.6. Circuit 5 (@base + 0280)

Address	Counter	Name	Type
@base + 0280	0	A_COINC_4_6	CED4_FPD6_coincidence_counter
@base + 0284	1	A_COINC_4_7	CED4_FPD7_coincidence_counter
@base + 0288	2	A_COINC_4_8	CED4_FPD8_coincidence_counter
@base + 028C	3	A_COINC_4_9	CED4_FPD9_coincidence_counter
@base + 0290	4	A_COINC_4_10	CED4_FPD10_coincidence_counter
@base + 0294	5	A_COINC_4_11	CED4_FPD11_coincidence_counter
@base + 0298	6	A_COINC_4_12	CED4_FPD12_coincidence_counter
@base + 029C	7	A_COINC_4_13	CED4_FPD13_coincidence_counter
@base + 02A0	8	A_COINC_5_0	CED5_FPD0_coincidence_counter
@base + 02A4	9	A_COINC_5_1	CED5_FPD1_coincidence_counter
@base + 02A8	10	A_COINC_5_2	CED5_FPD2_coincidence_counter
@base + 02AC	11	A_COINC_5_3	CED5_FPD3_coincidence_counter
@base + 02B0	12	A_COINC_5_4	CED5_FPD4_coincidence_counter
@base + 02B4	13	A_COINC_5_5	CED5_FPD5_coincidence_counter
@base + 02B8	14	A_COINC_5_6	CED5_FPD6_coincidence_counter
@base + 02BC	15	A_COINC_5_7	CED5_FPD7_coincidence_counter
@base + 02C0	16	A_COINC_5_8	CED5_FPD8_coincidence_counter
@base + 02C4	17	A_COINC_5_9	CED5_FPD9_coincidence_counter
@base + 02C8	18	A_COINC_5_10	CED5_FPD10_coincidence_counter
@base + 02CC	19	A_COINC_5_11	CED5_FPD11_coincidence_counter
@base + 02D0	20	A_COINC_5_12	CED5_FPD12_coincidence_counter
@base + 02D4	21	A_COINC_5_13	CED5_FPD13_coincidence_counter
@base + 02D8	22	A_COINC_6_0	CED6_FPD0_coincidence_counter
@base + 02DC	23	A_COINC_6_1	CED6_FPD1_coincidence_counter
@base + 02E0	24	A_COINC_6_2	CED6_FPD2_coincidence_counter
@base + 02E4	25	A_COINC_6_3	CED6_FPD3_coincidence_counter
@base + 02E8	26	A_COINC_6_4	CED6_FPD4_coincidence_counter
@base + 02EC	27	A_COINC_6_5	CED6_FPD5_coincidence_counter
@base + 02F0	28	A_COINC_6_6	CED6_FPD6_coincidence_counter
@base + 02F4	29	A_COINC_6_7	CED6_FPD7_coincidence_counter
@base + 02F8	30	A_COINC_6_8	CED6_FPD8_coincidence_counter
@base + 02FC	31	A_COINC_6_9	CED6_FPD9_coincidence_counter

4.3.7. Circuit 6 (@base + 0300)

Address	Counter	Name	Type
@base + 0300	0	A_COINC_6_10	CED6_FPD10_coincidence_counter
@base + 0304	1	A_COINC_6_11	CED6_FPD11_coincidence_counter
@base + 0308	2	A_COINC_6_12	CED6_FPD12_coincidence_counter
@base + 030C	3	A_COINC_6_13	CED6_FPD13_coincidence_counter
@base + 0310	4	A_COINC_7_0	CED7_FPD0_coincidence_counter
@base + 0314	5	A_COINC_7_1	CED7_FPD1_coincidence_counter
@base + 0318	6	A_COINC_7_2	CED7_FPD2_coincidence_counter
@base + 031C	7	A_COINC_7_3	CED7_FPD3_coincidence_counter
@base + 0320	8	A_COINC_7_4	CED7_FPD4_coincidence_counter
@base + 0324	9	A_COINC_7_5	CED7_FPD5_coincidence_counter
@base + 0328	10	A_COINC_7_6	CED7_FPD6_coincidence_counter
@base + 032C	11	A_COINC_7_7	CED7_FPD7_coincidence_counter
@base + 0330	12	A_COINC_7_8	CED7_FPD8_coincidence_counter
@base + 0334	13	A_COINC_7_9	CED7_FPD9_coincidence_counter
@base + 0338	14	A_COINC_7_10	CED7_FPD10_coincidence_counter
@base + 033C	15	A_COINC_7_11	CED7_FPD11_coincidence_counter
@base + 0340	16	A_COINC_7_12	CED7_FPD12_coincidence_counter
@base + 0344	17	A_COINC_7_13	CED7_FPD13_coincidence_counter
@base + 0348	18	A_COINC_8_0	CED8_FPD0_coincidence_counter
@base + 034C	19	A_COINC_8_1	CED8_FPD1_coincidence_counter
@base + 0350	20	A_COINC_8_2	CED8_FPD2_coincidence_counter
@base + 0354	21	A_COINC_8_3	CED8_FPD3_coincidence_counter
@base + 0358	22	A_COINC_8_4	CED8_FPD4_coincidence_counter
@base + 035C	23	A_COINC_8_5	CED8_FPD5_coincidence_counter
@base + 0360	24	A_COINC_8_6	CED8_FPD6_coincidence_counter
@base + 0364	25	A_COINC_8_7	CED8_FPD7_coincidence_counter
@base + 0368	26	A_COINC_8_8	CED8_FPD8_coincidence_counter
@base + 036C	27	A_COINC_8_9	CED8_FPD9_coincidence_counter
@base + 0370	28	A_COINC_8_10	CED8_FPD10_coincidence_counter
@base + 0374	29	A_COINC_8_11	CED8_FPD11_coincidence_counter
@base + 0378	30	A_COINC_8_12	CED8_FPD12_coincidence_counter
@base + 037C	31	A_COINC_8_13	CED8_FPD13_coincidence_counter

4.3.8. Circuit 7 (@base + 0380)

Address	Counter	Name	Type
@base + 0380	0	A_NCCED0	CED0 Direct Counter
@base + 0384	1	A_NCCED1	CED1 Direct Counter
@base + 0388	2	A_NCCED2	CED2 Direct Counter
@base + 038C	3	A_NCCED3	CED3 Direct Counter
@base + 0390	4	A_NCCED4	CED4 Direct Counter
@base + 0394	5	A_NCCED5	CED5 Direct Counter
@base + 0398	6	A_NCCED6	CED6 Direct Counter
@base + 039C	7	A_NCCED7	CED7 Direct Counter
@base + 03A0	8	A_NCCED8	CED8 Direct Counter
@base + 03A4	9	A_NCFPD0	FPD0 Direct Counter
@base + 03A8	10	A_NCFPD1	FPD1 Direct Counter
@base + 03AC	11	A_NCFPD2	FPD2 Direct Counter
@base + 03B0	12	A_NCFPD3	FPD3 Direct Counter
@base + 03B4	13	A_NCFPD4	FPD4 Direct Counter
@base + 03B8	14	A_NCFPD5	FPD5 Direct Counter
@base + 03BC	15	A_NCFPD6	FPD6 Direct Counter
@base + 03C0	16	A_NCFPD7	FPD7 Direct Counter
@base + 03C4	17	A_NCFPD8	FPD8 Direct Counter
@base + 03C8	18	A_NCFPD9	FPD9 Direct Counter
@base + 03CC	19	A_NCFPD10	FPD10 Direct Counter
@base + 03D0	20	A_NCFPD11	FPD11 Direct Counter
@base + 03D4	21	A_NCFPD12	FPD12 Direct Counter
@base + 03D8	22	A_NCFPD13	FPD13 Direct Counter
@base + 03DC	23	NB_VALID	Number of VALID signal in the cycle (/VALID)
@base + 03E0	24	*Non available*	
@base + 03E4	25	*Non available*	
@base + 03E8	26	*Non available*	
@base + 03EC	27	*Non available*	
@base + 03F0	28	*Non available*	
@base + 03F4	29	*Non available*	
@base + 03F8	30	*Non available*	
@base + 03FC	31	*Non available*	

4.3.9. Circuit 8 (@base + 0800)

Address	Counter	Name	Type
@base + 0800	0	*Non available*	
@base + 0804	1	*Non available*	
@base + 0808	2	*Non available*	
@base + 080C	3	*Non available*	
@base + 0810	4	*Non available*	
@base + 0814	5	*Non available*	
@base + 0818	6	B_CCED0	CED0 Non Conditioned Direct Counter
@base + 081C	7	B_CCED1	CED1 Non Conditioned Direct Counter
@base + 0820	8	B_CCED2	CED2 Non Conditioned Direct Counter
@base + 0824	9	B_CCED3	CED3 Non Conditioned Direct Counter
@base + 0828	10	B_CCED4	CED4 Non Conditioned Direct Counter
@base + 082C	11	B_CCED5	CED5 Non Conditioned Direct Counter
@base + 0830	12	B_CCED6	CED6 Non Conditioned Direct Counter
@base + 0834	13	B_CCED7	CED7 Non Conditioned Direct Counter
@base + 0838	14	B_CCED8	CED8 Non Conditioned Direct Counter
@base + 083C	15	B_CFPD0	FPD0 Non Conditioned Direct Counter
@base + 0840	16	B_CFPD1	FPD1 Non Conditioned Direct Counter
@base + 0844	17	B_CFPD2	FPD2 Non Conditioned Direct Counter
@base + 0848	18	B_CFPD3	FPD3 Non Conditioned Direct Counter
@base + 084C	19	B_CFPD4	FPD4 Non Conditioned Direct Counter
@base + 0850	20	B_CFPD5	FPD5 Non Conditioned Direct Counter
@base + 0854	21	B_CFPD6	FPD6 Non Conditioned Direct Counter
@base + 0858	22	B_CFPD7	FPD7 Non Conditioned Direct Counter
@base + 085C	23	B_CFPD8	FPD8 Non Conditioned Direct Counter
@base + 0860	24	B_CFPD9	FPD9 Non Conditioned Direct Counter
@base + 0864	25	B_CFPD10	FPD10 Non Conditioned Direct Counter
@base + 0868	26	B_CFPD11	FPD11 Non Conditioned Direct Counter
@base + 086C	27	B_CFPD12	FPD12 Non Conditioned Direct Counter
@base + 0870	28	B_CFPD13	FPD13 Non Conditioned Direct Counter
@base + 0874	29	*Non available*	
@base + 0878	30	*Non available*	
@base + 087C	31	*Non available*	

4.3.10. Circuit 9 (@base + 0880)

Address	Counter	Name	Type
@base + 0880	0	B_CC3	CED3 Conditioned Direct Counter
@base + 0884	1	B_CC4	CED4 Conditioned Direct Counter
@base + 0888	2	B_CC5	CED5 Conditioned Direct Counter
@base + 088C	3	B_CC6	CED6 Conditioned Direct Counter
@base + 0890	4	B_CC7	CED7 Conditioned Direct Counter
@base + 0894	5	B_CC8	CED8 Conditioned Direct Counter
@base + 0898	6	B_CF0	FPD0 Conditioned Direct Counter
@base + 089C	7	B_CF1	FPD1 Conditioned Direct Counter
@base + 08A0	8	B_CF2	FPD2 Conditioned Direct Counter
@base + 08A4	9	B_CF3	FPD3 Conditioned Direct Counter
@base + 08A8	10	B_CF4	FPD4 Conditioned Direct Counter
@base + 08AC	11	B_CF5	FPD5 Conditioned Direct Counter
@base + 08B0	12	B_CF6	FPD6 Conditioned Direct Counter
@base + 08B4	13	B_CF7	FPD7 Conditioned Direct Counter
@base + 08B8	14	B_CF8	FPD8 Conditioned Direct Counter
@base + 08BC	15	B_CF9	FPD9 Conditioned Direct Counter
@base + 08C0	16	B_CF10	FPD10 Conditioned Direct Counter
@base + 08C4	17	B_CF11	FPD11 Conditioned Direct Counter
@base + 08C8	18	B_CF12	FPD12 Conditioned Direct Counter
@base + 08CC	19	B_CF13	FPD13 Conditioned Direct Counter
@base + 08D0	20	B_M12_C0	CED0 Multihit_12_ counter (CED0 and 2 FPD)
@base + 08D4	21	B_M12_C1	CED1 Multihit_12_counter (CED1 and 2 FPD)
@base + 08D8	22	B_M12_C2	CED2 Multihit_12_counter (CED2 and 2 FPD)
@base + 08DC	23	B_M12_C3	CED3 Multihit_12_counter (CED3 and 2 FPD)
@base + 08E0	24	B_M12_C4	CED4 Multihit_12_counter (CED4 and 2 FPD)
@base + 08E4	25	B_M12_C5	CED5 Multihit_12_counter (CED5 and 2 FPD)
@base + 08E8	26	B_M12_C6	CED6 Multihit_12_counter (CED6 and 2 FPD)
@base + 08EC	27	B_M12_C7	CED7 Multihit_12_counter (CED7 and 2 FPD)
@base + 08F0	28	B_M12_C8	CED8 Multihit_12_counter (CED8 and 2 FPD)
@base + 08F4	29	B_M12_F0	FPD0 Multihit_12_counter (PFD0 and 2 CED)
@base + 08F8	30	B_M12_F1	FPD1 Multihit_12_counter (PFD1 and 2 CED)
@base + 08FC	31	B_M12_F2	FPD2 Multihit_12_counter (PFD2 and 2 CED)

4.3.11. Circuit 10 (@base + 0900)

Address	Counter	Name	Type
@base + 0900	0	B_M12_F3	FPD3 Multihit_12_counter (PFD3 and 2 CED)
@base + 0904	1	B_M12_F4	FPD4 Multihit_12_counter (PFD4 and 2 CED)
@base + 0908	2	B_M12_F5	FPD5 Multihit_12_counter (PFD5 and 2 CED)
@base + 090C	3	B_M12_F6	FPD6 Multihit_12_counter (PFD6 and 2 CED)
@base + 0910	4	B_M12_F7	FPD7 Multihit_12_counter (PFD7 and 2 CED)
@base + 0914	5	B_M12_F8	FPD8 Multihit_12_counter (PFD8 and 2 CED)
@base + 0918	6	B_M12_F9	FPD9 Multihit_12_counter (PFD9 and 2 CED)
@base + 091C	7	B_M12_F10	FPD10 Multihit_12_counter (PFD10 and 2 CED)
@base + 0920	8	B_M12_F11	FPD11 Multihit_12_counter (PFD11 and 2 CED)
@base + 0924	9	B_M12_F12	FPD12 Multihit_12_counter (PFD12 and 2 CED)
@base + 0928	10	B_M12_F13	FPD13 Multihit_12_counter (PFD13 and 2 CED)
@base + 092C	11	B_M22_C0	CED0 Multihit_22_counter (CED0 and MULTI ≥ 3)
@base + 0930	12	B_M22_C1	CED1 Multihit_22_counter (CED1 and MULTI ≥ 3)
@base + 0934	13	B_M22_C2	CED2 Multihit_22_counter (CED2 and MULTI ≥ 3)
@base + 0938	14	B_M22_C3	CED3 Multihit_22_counter (CED3 and MULTI ≥ 3)
@base + 093C	15	B_M22_C4	CED4 Multihit_22_counter (CED4 and MULTI ≥ 3)
@base + 0940	16	B_M22_C5	CED5 Multihit_22_counter (CED5 and MULTI ≥ 3)
@base + 0944	17	B_M22_C6	CED6 Multihit_22_counter (CED6 and MULTI ≥ 3)
@base + 0948	18	B_M22_C7	CED7 Multihit_22_counter (CED7 and MULTI ≥ 3)
@base + 094C	19	B_M22_C8	CED8 Multihit_22_counter (CED8 and MULTI ≥ 3)
@base + 0950	20	B_M22_F0	FPD0 Multihit_22_counter (FPD0 and MULTI ≥ 3)
@base + 0954	21	B_M22_F1	FPD1 Multihit_22_counter (FPD1 and MULTI ≥ 3)
@base + 0958	22	B_M22_F2	FPD2 Multihit_22_counter (FPD2 and MULTI ≥ 3)
@base + 095C	23	B_M22_F3	FPD3 Multihit_22_counter (FPD3 and MULTI ≥ 3)
@base + 0960	24	B_M22_F4	FPD4 Multihit_22_counter (FPD4 and MULTI ≥ 3)
@base + 0964	25	B_M22_F5	FPD5 Multihit_22_counter (FPD5 and MULTI ≥ 3)
@base + 0968	26	B_M22_F6	FPD6 Multihit_22_counter (FPD6 and MULTI ≥ 3)
@base + 096C	27	B_M22_F7	FPD7 Multihit_22_counter (FPD7 and MULTI ≥ 3)
@base + 0970	28	B_M22_F8	FPD8 Multihit_22_counter (FPD8 and MULTI ≥ 3)
@base + 0974	29	B_M22_F9	FPD9 Multihit_22_counter (FPD9 and MULTI ≥ 3)
@base + 0978	30	B_M22_F10	FPD10 Multihit_22_counter (FPD10 and MULTI ≥ 3)
@base + 097C	31	B_M22_F11	FPD11 Multihit_22_counter (FPD11 and MULTI ≥ 3)

4.3.12. Circuit 11 (@base + 0980)

Address	Counter	Name	Type
@base + 0980	0	B_M22_F12	FPD12 Multihit_22_counter (FPD12 and MULTI ≥ 3)
@base + 0984	1	B_M22_F13	FPD13 Multihit_22_counter (FPD13 and MULTI ≥ 3)
@base + 0988	2	B_COINC_0_0	CED0_FPD0_coincidence_counter
@base + 098C	3	B_COINC_0_1	CED0_FPD1_coincidence_counter
@base + 0990	4	B_COINC_0_2	CED0_FPD2_coincidence_counter
@base + 0994	5	B_COINC_0_3	CED0_FPD3_coincidence_counter
@base + 0998	6	B_COINC_0_4	CED0_FPD4_coincidence_counter
@base + 099C	7	B_COINC_0_5	CED0_FPD5_coincidence_counter
@base + 09A0	8	B_COINC_0_6	CED0_FPD6_coincidence_counter
@base + 09A4	9	B_COINC_0_7	CED0_FPD7_coincidence_counter
@base + 09A8	10	B_COINC_0_8	CED0_FPD8_coincidence_counter
@base + 09AC	11	B_COINC_0_9	CED0_FPD9_coincidence_counter
@base + 09B0	12	B_COINC_0_10	CED0_FPD10_coincidence_counter
@base + 09B4	13	B_COINC_0_11	CED0_FPD11_coincidence_counter
@base + 09B8	14	B_COINC_0_12	CED0_FPD12_coincidence_counter
@base + 09BC	15	B_COINC_0_13	CED0_FPD13_coincidence_counter
@base + 09C0	16	B_COINC_1_0	CED1_FPD0_coincidence_counter
@base + 09C4	17	B_COINC_1_1	CED1_FPD1_coincidence_counter
@base + 09C8	18	B_COINC_1_2	CED1_FPD2_coincidence_counter
@base + 09CC	19	B_COINC_1_3	CED1_FPD3_coincidence_counter
@base + 09D0	20	B_COINC_1_4	CED1_FPD4_coincidence_counter
@base + 09D4	21	B_COINC_1_5	CED1_FPD5_coincidence_counter
@base + 09D8	22	B_COINC_1_6	CED1_FPD6_coincidence_counter
@base + 09DC	23	B_COINC_1_7	CED1_FPD7_coincidence_counter
@base + 09E0	24	B_COINC_1_8	CED1_FPD8_coincidence_counter
@base + 09E4	25	B_COINC_1_9	CED1_FPD9_coincidence_counter
@base + 09E8	26	B_COINC_1_10	CED1_FPD10_coincidence_counter
@base + 09EC	27	B_COINC_1_11	CED1_FPD11_coincidence_counter
@base + 09F0	28	B_COINC_1_12	CED1_FPD12_coincidence_counter
@base + 09F4	29	B_COINC_1_13	CED1_FPD13_coincidence_counter
@base + 09F8	30	B_COINC_2_0	CED2_FPD0_coincidence_counter
@base + 09FC	31	B_COINC_2_1	CED2_FPD1_coincidence_counter

4.3.13. Circuit 12 (@base + 0A00)

Address	Counter	Name	Type
@base + 0A00	0	B_COINC_2_2	CED2_FPD2_coincidence_counter
@base + 0A04	1	B_COINC_2_3	CED2_FPD3_coincidence_counter
@base + 0A08	2	B_COINC_2_4	CED2_FPD4_coincidence_counter
@base + 0A0C	3	B_COINC_2_5	CED2_FPD5_coincidence_counter
@base + 0A10	4	B_COINC_2_6	CED2_FPD6_coincidence_counter
@base + 0A14	5	B_COINC_2_7	CED2_FPD7_coincidence_counter
@base + 0A18	6	B_COINC_2_8	CED2_FPD8_coincidence_counter
@base + 0A1C	7	B_COINC_2_9	CED2_FPD9_coincidence_counter
@base + 0A20	8	B_COINC_2_10	CED2_FPD10_coincidence_counter
@base + 0A24	9	B_COINC_2_11	CED2_FPD11_coincidence_counter
@base + 0A28	10	B_COINC_2_12	CED2_FPD12_coincidence_counter
@base + 0A2C	11	B_COINC_2_13	CED2_FPD13_coincidence_counter
@base + 0A30	12	B_COINC_3_0	CED3_FPD0_coincidence_counter
@base + 0A34	13	B_COINC_3_1	CED3_FPD1_coincidence_counter
@base + 0A38	14	B_COINC_3_2	CED3_FPD2_coincidence_counter
@base + 0A3C	15	B_COINC_3_3	CED3_FPD3_coincidence_counter
@base + 0A40	16	B_COINC_3_4	CED3_FPD4_coincidence_counter
@base + 0A44	17	B_COINC_3_5	CED3_FPD5_coincidence_counter
@base + 0A48	18	B_COINC_3_6	CED3_FPD6_coincidence_counter
@base + 0A4C	19	B_COINC_3_7	CED3_FPD7_coincidence_counter
@base + 0A50	20	B_COINC_3_8	CED3_FPD8_coincidence_counter
@base + 0A54	21	B_COINC_3_9	CED3_FPD9_coincidence_counter
@base + 0A58	22	B_COINC_3_10	CED3_FPD10_coincidence_counter
@base + 0A5C	23	B_COINC_3_11	CED3_FPD11_coincidence_counter
@base + 0A60	24	B_COINC_3_12	CED3_FPD12_coincidence_counter
@base + 0A64	25	B_COINC_3_13	CED3_FPD13_coincidence_counter
@base + 0A68	26	B_COINC_4_0	CED4_FPD0_coincidence_counter
@base + 0A6C	27	B_COINC_4_1	CED4_FPD1_coincidence_counter
@base + 0A70	28	B_COINC_4_2	CED4_FPD2_coincidence_counter
@base + 0A74	29	B_COINC_4_3	CED4_FPD3_coincidence_counter
@base + 0A78	30	B_COINC_4_4	CED4_FPD4_coincidence_counter
@base + 0A7C	31	B_COINC_4_5	CED4_FPD5_coincidence_counter

4.3.14. Circuit 13 (@base + 0A80)

Address	Counter	Name	Type
@base + 0A80	0	B_COINC_4_6	CED4_FPD6_coincidence_counter
@base + 0A84	1	B_COINC_4_7	CED4_FPD7_coincidence_counter
@base + 0A88	2	B_COINC_4_8	CED4_FPD8_coincidence_counter
@base + 0A8C	3	B_COINC_4_9	CED4_FPD9_coincidence_counter
@base + 0A90	4	B_COINC_4_10	CED4_FPD10_coincidence_counter
@base + 0A94	5	B_COINC_4_11	CED4_FPD11_coincidence_counter
@base + 0A98	6	B_COINC_4_12	CED4_FPD12_coincidence_counter
@base + 0A9C	7	B_COINC_4_13	CED4_FPD13_coincidence_counter
@base + 0AA0	8	B_COINC_5_0	CED5_FPD0_coincidence_counter
@base + 0AA4	9	B_COINC_5_1	CED5_FPD1_coincidence_counter
@base + 0AA8	10	B_COINC_5_2	CED5_FPD2_coincidence_counter
@base + 0AAC	11	B_COINC_5_3	CED5_FPD3_coincidence_counter
@base + 0AB0	12	B_COINC_5_4	CED5_FPD4_coincidence_counter
@base + 0AB4	13	B_COINC_5_5	CED5_FPD5_coincidence_counter
@base + 0AB8	14	B_COINC_5_6	CED5_FPD6_coincidence_counter
@base + 0ABC	15	B_COINC_5_7	CED5_FPD7_coincidence_counter
@base + 0AC0	16	B_COINC_5_8	CED5_FPD8_coincidence_counter
@base + 0AC4	17	B_COINC_5_9	CED5_FPD9_coincidence_counter
@base + 0AC8	18	B_COINC_5_10	CED5_FPD10_coincidence_counter
@base + 0ACC	19	B_COINC_5_11	CED5_FPD11_coincidence_counter
@base + 0AD0	20	B_COINC_5_12	CED5_FPD12_coincidence_counter
@base + 0AD4	21	B_COINC_5_13	CED5_FPD13_coincidence_counter
@base + 0AD8	22	B_COINC_6_0	CED6_FPD0_coincidence_counter
@base + 0ADC	23	B_COINC_6_1	CED6_FPD1_coincidence_counter
@base + 0AE0	24	B_COINC_6_2	CED6_FPD2_coincidence_counter
@base + 0AE4	25	B_COINC_6_3	CED6_FPD3_coincidence_counter
@base + 0AE8	26	B_COINC_6_4	CED6_FPD4_coincidence_counter
@base + 0AEC	27	B_COINC_6_5	CED6_FPD5_coincidence_counter
@base + 0AF0	28	B_COINC_6_6	CED6_FPD6_coincidence_counter
@base + 0AF4	29	B_COINC_6_7	CED6_FPD7_coincidence_counter
@base + 0AF8	30	B_COINC_6_8	CED6_FPD8_coincidence_counter
@base + 0AFC	31	B_COINC_6_9	CED6_FPD9_coincidence_counter

4.3.15. Circuit 14 (@base + 0B00)

Address	Counter	Name	Type
@base + 0B00	0	B_COINC_6_10	CED6_FPD10_coincidence_counter
@base + 0B04	1	B_COINC_6_11	CED6_FPD11_coincidence_counter
@base + 0B08	2	B_COINC_6_12	CED6_FPD12_coincidence_counter
@base + 0B0C	3	B_COINC_6_13	CED6_FPD13_coincidence_counter
@base + 0B10	4	B_COINC_7_0	CED7_FPD0_coincidence_counter
@base + 0B14	5	B_COINC_7_1	CED7_FPD1_coincidence_counter
@base + 0B18	6	B_COINC_7_2	CED7_FPD2_coincidence_counter
@base + 0B1C	7	B_COINC_7_3	CED7_FPD3_coincidence_counter
@base + 0B20	8	B_COINC_7_4	CED7_FPD4_coincidence_counter
@base + 0B24	9	B_COINC_7_5	CED7_FPD5_coincidence_counter
@base + 0B28	10	B_COINC_7_6	CED7_FPD6_coincidence_counter
@base + 0B2C	11	B_COINC_7_7	CED7_FPD7_coincidence_counter
@base + 0B30	12	B_COINC_7_8	CED7_FPD8_coincidence_counter
@base + 0B34	13	B_COINC_7_9	CED7_FPD9_coincidence_counter
@base + 0B38	14	B_COINC_7_10	CED7_FPD10_coincidence_counter
@base + 0B3C	15	B_COINC_7_11	CED7_FPD11_coincidence_counter
@base + 0B40	16	B_COINC_7_12	CED7_FPD12_coincidence_counter
@base + 0B44	17	B_COINC_7_13	CED7_FPD13_coincidence_counter
@base + 0B48	18	B_COINC_8_0	CED8_FPD0_coincidence_counter
@base + 0B4C	19	B_COINC_8_1	CED8_FPD1_coincidence_counter
@base + 0B50	20	B_COINC_8_2	CED8_FPD2_coincidence_counter
@base + 0B54	21	B_COINC_8_3	CED8_FPD3_coincidence_counter
@base + 0B58	22	B_COINC_8_4	CED8_FPD4_coincidence_counter
@base + 0B5C	23	B_COINC_8_5	CED8_FPD5_coincidence_counter
@base + 0B60	24	B_COINC_8_6	CED8_FPD6_coincidence_counter
@base + 0B64	25	B_COINC_8_7	CED8_FPD7_coincidence_counter
@base + 0B68	26	B_COINC_8_8	CED8_FPD8_coincidence_counter
@base + 0B6C	27	B_COINC_8_9	CED8_FPD9_coincidence_counter
@base + 0B70	28	B_COINC_8_10	CED8_FPD10_coincidence_counter
@base + 0B74	29	B_COINC_8_11	CED8_FPD11_coincidence_counter
@base + 0B78	30	B_COINC_8_12	CED8_FPD12_coincidence_counter
@base + 0B7C	31	B_COINC_8_13	CED8_FPD13_coincidence_counter

4.3.16. Circuit 15 (@base + 0B80)

Address	Counter	Name	Type
@base + 0B80	0	B_NCCED0	CED0 Direct Counter
@base + 0B84	1	B_NCCED1	CED1 Direct Counter
@base + 0B88	2	B_NCCED2	CED2 Direct Counter
@base + 0B8C	3	B_NCCED3	CED3 Direct Counter
@base + 0B90	4	B_NCCED4	CED4 Direct Counter
@base + 0B94	5	B_NCCED5	CED5 Direct Counter
@base + 0B98	6	B_NCCED6	CED6 Direct Counter
@base + 0B9C	7	B_NCCED7	CED7 Direct Counter
@base + 0BA0	8	B_NCCED8	CED8 Direct Counter
@base + 0BA4	9	B_NCFPD0	FPD0 Direct Counter
@base + 0BA8	10	B_NCFPD1	FPD1 Direct Counter
@base + 0BAC	11	B_NCFPD2	FPD2 Direct Counter
@base + 0BB0	12	B_NCFPD3	FPD3 Direct Counter
@base + 0BB4	13	B_NCFPD4	FPD4 Direct Counter
@base + 0BB8	14	B_NCFPD5	FPD5 Direct Counter
@base + 0BBC	15	B_NCFPD6	FPD6 Direct Counter
@base + 0BC0	16	B_NCFPD7	FPD7 Direct Counter
@base + 0BC4	17	B_NCFPD8	FPD8 Direct Counter
@base + 0BC8	18	B_NCFPD9	FPD9 Direct Counter
@base + 0BCC	19	B_NCFPD10	FPD10 Direct Counter
@base + 0BD0	20	B_NCFPD11	FPD11 Direct Counter
@base + 0BD4	21	B_NCFPD12	FPD12 Direct Counter
@base + 0BD8	22	B_NCFPD13	FPD13 Direct Counter
@base + 0BDC	23	NB_BPO	Number of BPO signal in the cycle
@base + 0BE0	24	*Non available*	
@base + 0BE4	25	*Non available*	
@base + 0BE8	26	*Non available*	
@base + 0BEC	27	*Non available*	
@base + 0BF0	28	*Non available*	
@base + 0BF4	29	*Non available*	
@base + 0BF8	30	*Non available*	
@base + 0BFC	31	*Non available*	

4.3.17. Circuit 16 (@base + 1000)

Address	Counter	Name	Type
@base + 1000	0	A_CC0	CED0 Conditioned Direct Counter (side A)
@base + 1004	1	A_CC1	CED1 Conditioned Direct Counter (side A)
@base + 1008	2	A_CC2	CED2 Conditioned Direct Counter (side A)
@base + 100C	3	B_CC0	CED0 Conditioned Direct Counter (side B)
@base + 1010	4	B_CC1	CED1 Conditioned Direct Counter (side B)
@base + 1014	5	B_CC2	CED2 Conditioned Direct Counter (side B)
@base + 1018	6	*Non available*	
@base + 101C	7	*Non available*	
@base + 1020	8	*Non available*	
@base + 1024	9	*Non available*	
@base + 1028	10	*Non available*	
@base + 102C	11	*Non available*	
@base + 1030	12	*Non available*	
@base + 1034	13	*Non available*	
@base + 1038	14	*Non available*	
@base + 103C	15	*Non available*	
@base + 1040	16	*Non available*	
@base + 1044	17	*Non available*	
@base + 1048	18	*Non available*	
@base + 104C	19	*Non available*	
@base + 1050	20	*Non available*	
@base + 1054	21	*Non available*	
@base + 1058	22	*Non available*	
@base + 105C	23	*Non available*	
@base + 1060	24	*Non available*	
@base + 1064	25	*Non available*	
@base + 1068	26	*Non available*	
@base + 106C	27	*Non available*	
@base + 1070	28	*Non available*	
@base + 1074	29	*Non available*	
@base + 1078	30	*Non available*	
@base + 107C	31	*Non available*	

5. Address Map

5.1. Space counters

Address	Selection	type	Comment
Octant 0			
@base	/COUNT0	Counters	Non available counters
@base + 18h	/COUNT0	Counters	A_CCED[8..0], A_CFPD[13..0]
@base + 80h	/COUNT1	Counters	A_CC[8..3], A_CF[13..0], A_M12_C[8..0], A_M12_F[2..0]
@base + 100h	/COUNT2	Counters	A_M12_F[13..3], A_M22_C[8..0], A_M22_F[11..0]
@base + 180h	/COUNT3	Counters	A_M22_F[13..12], A_COINC_0_[13..0], A_COINC_1_[13..0], A_COINC_2_[1..0]
@base + 200h	/COUNT4	Counters	A_COINC_2_[13..2], A_COINC_3_[13..0], A_COINC_4_[5..0]
@base + 280h	/COUNT5	Counters	A_COINC_4_[13..6], A_COINC_5_[13..0], A_COINC_6_[9..0]
@base + 300h	/COUNT6	Counters	A_COINC_6_[13..10], A_COINC_7_[13..0], A_COINC_8_[13..0]
@base + 380h	/COUNT7	Counters	A_NCCED[8..0], A_NCFPD[13..0]
@base + 3DCh	/COUNT7	Counters	Non available counters
@base + 1000h	/PIGGY	Counters	A_CC[2..0] (counter 0 to 2)
@base + 400h	/COUNT0	Registers	See the COUNT32 ASIC component documentation
@base + 480h	/COUNT1	Registers	See the COUNT32 ASIC component documentation
@base + 500h	/COUNT2	Registers	See the COUNT32 ASIC component documentation
@base + 580h	/COUNT3	Registers	See the COUNT32 ASIC component documentation
@base + 600h	/COUNT4	Registers	See the COUNT32 ASIC component documentation
@base + 680h	/COUNT5	Registers	See the COUNT32 ASIC component documentation
@base + 700h	/COUNT6	Registers	See the COUNT32 ASIC component documentation
@base + 780h	/COUNT7	Registers	See the COUNT32 ASIC component documentation
@base + 1400h	/PIGGY	Registers	See the COUNT32 ASIC component documentation
Octant 1			
@base + 800h	/COUNT8	Counters	Non available counters
@base + 818h	/COUNT8	Counters	B_CCED[8..0], B_CFPD[13..0], B_CC[2..0]
@base + 880h	/COUNT9	Counters	B_CC[8..3], B_CF[13..0], B_M12_C[8..0], B_M12_F[2..0]
@base + 900h	/COUNT10	Counters	B_M12_F[13..3], B_M22_C[8..0], B_M22_F[11..0]
@base + 980h	/COUNT11	Counters	B_M22_F[13..12], B_COINC_0_[13..0], B_COINC_1_[13..0], B_COINC_2_[1..0]

Address	Selection	type	Comment
@base + A00h	/COUNT12	Counters	B_COINC_2_[13..2], B_COINC_3_[13..0], B_COINC_4_[5..0]
@base + A80h	/COUNT13	Counters	B_COINC_4_[13..6], B_COINC_5_[13..0], B_COINC_6_[9..0]
@base + B00h	/COUNT14	Counters	B_COINC_6_[13..10], B_COINC_7_[13..0], B_COINC_8_[13..0]
@base + B80h	/COUNT15	Counters	B_NCCED[8..0], B_NCFPD[13..0]
@base + BDCh	/COUNT15	Counters	Non available counters
@base + 1000h	/PIGGY	Counters	B_CC[2..0] (counter 3 to 5)
@base + C00h	/COUNT8	Registers	See the COUNT32 ASIC component documentation
@base + C80h	/COUNT9	Registers	See the COUNT32 ASIC component documentation
@base + D00h	/COUNT10	Registers	See the COUNT32 ASIC component documentation
@base + D80h	/COUNT11	Registers	See the COUNT32 ASIC component documentation
@base + E00h	/COUNT12	Registers	See the COUNT32 ASIC component documentation
@base + E80h	/COUNT13	Registers	See the COUNT32 ASIC component documentation
@base + F00h	/COUNT14	Registers	See the COUNT32 ASIC component documentation
@base + F80h	/COUNT15	Registers	See the COUNT32 ASIC component documentation
@base + 1400h	/PIGGY	Registers	See the COUNT32 ASIC component documentation

5.2. Board Space registers

@base +	label	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
1800	DCOINC	R/W	DCOINC[15..0]															
1804	ETAT	W			ETAT[13]	ETAT[12]	ETAT[11]	VAL_COM	ETAT[9]	ETAT[8]	ETAT[7]	ETAT[6]	ETAT[5]	ETAT[4]	ETAT[3]	ETAT[2]	ETAT[1]	ETAT[0]
		R	0	0	ETAT[13]	ETAT[12]	ETAT[11]	V_COM	ETAT[9]	ETAT[8]	ETAT[7]	ETAT[6]	ETAT[5]	ETAT[4]	ETAT[3]	ETAT[2]	ETAT[1]	ETAT[0]
1880	IT	W										INT3	INT2	INT1			V_IRQ	
		R	0	0	0	0	0	0	0	0	0	INT3	INT2	INT1	0	0	V_IRQ	IT
1884	CHOIX	W															CHOIX1	CHOIX0
		R	0	0	0	0	0	0	0	0	0	0	0	0	0	VCOINC	CHOIX1	CHOIX0
1900	DELAY	W									DELAY[7..0]							

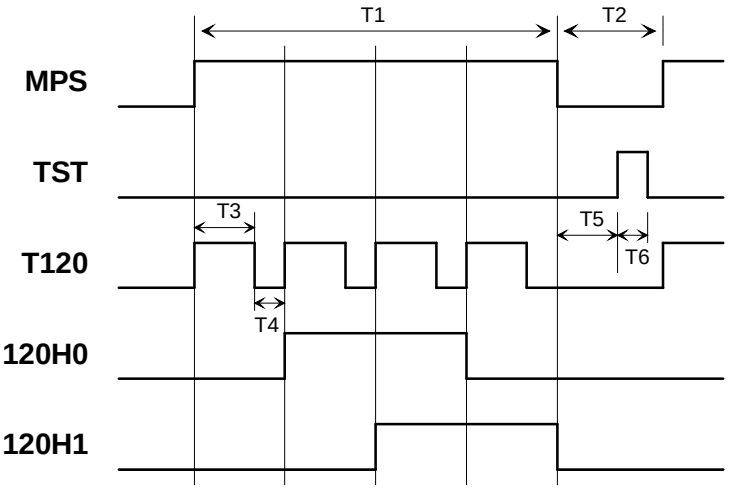
The high significant bit (D[31..16]) are not significant, there are not represent in this table.

6. User signals present on the VXI connectors

The following signals are present on the VXI connectors **only if** the Interface Box board are present in the crate.

VXI line	Pin Number	Name	Function
ECLTRG0	A1	HF	Beam Pulse Frequency (ECL level)
ECLTRG1	A3	/HF	Beam Pulse Frequency (ECL level)
TTLTRG0	A23	/MPS	Macro Pulse Signal (TTL level)
TTLTRG1	C23	120H0	120 Hz slicing, code 0 (TTL level)
TTLTRG2	A24	120H1	120 Hz slicing, code 1 (TTL level)
TTLTRG3	C24	T120	120 Hz Trigger (TTL level)
TTLTRG4	A26	/MRUN	Master Run (TTL level)
TTLTRG5	C26	DHF	Delayed Beam Pulse Frequency (TTL level)
TTLTRG6	A27	/MRST	Master Reset (TTL level)
TTLTRG7	C27	LTPO	Laser Time Pick off (TTL level)
SUMBUS	A32	TST	Laser / Generator Trigger
Local bus 09	A18 – C18	HEL	HELICITY
Local bus 10	A20 – C20	QRT	Quartet
Local bus 11	A21 – C21	-	Reserved

HF, /HF :	Beam reference (32 ns period)
/MPS :	Macro pulse Synchronization (33 ms period)
120H0, 120H1 :	120 Hz slices code
T120 :	120 Hz trigger (8 ms period)
/MRUN :	Master Run (enable data acquisition of all DMCH-16X modules
DHF :	Delayed beam reference (34 ns period)
/MRST :	Master RESET (Residual data deletion in all DMCH-16X modules)
LTPO :	Laser Time Pick Off
HEL :	HELICITY direction
QRT :	Quartet Trigger
TST :	Time Gate for generator or laser control



With :

T1 :	1/30 S
T2 :	200 µS
T3 + T4 :	1/120 S
T4 :	3 µS
T5 :	130 µS
T6 :	1 µS

Figure 6 : VXI user signals waveform

7. Consumption

7.1. CEDFPD20 circuits Power consumption (ALTERA EPM7512AE) :

The power consumption can be calculated with the following formula :

$$P = Pint + Pio = Iccint \times Vcc + Pio$$

With Pint = integrate circuit core power consumption
Iccint = integrate circuit core current
Pio = power consumption of the input/output pads

7.1.1. Power consumption of the core component

The value Iccint can be calculate with the following formula :

$$Iccint = (0,71 \times MC_{TON}) + (0,30 \times (MC_{DEV} - MC_{TON})) + (0,014 \times MC_{USED} \times F_{MAX} \times TOG_{LC})$$

With MC_{TON} : Number of macrocell with the « TURBO BIT « option
MC_{DEV} : Number of macrocell into the component
MC_{USED} : Number of macrocell used in the design
F_{MAX} : Clock Frequency used in the design (in MHz)
TOG_{LC} : Percentage of cell changing state at each clock edge (typ. 12,5%)

After definition and simulation of the FPGA content the applicable parameters are :
MC_{TON} : 241
MC_{DEV} : 512
MC_{USED} : 241

7.1.1.1. Maximum frequency definition :

The maximum frequency c an be define as been the invert of the time between the BPO2 signal (sample signal of the outputs) and the BPO1 signal (reset signal of the output flip flops) :

$$T = 12 \text{ nS} \Rightarrow F_{MAX} = (1/12) * 10^{-9} = \mathbf{83 \text{ MHz} = F_{MAX}}$$

7.1.1.2. Maximum number of cell which change state on the BPO2 signal rising edge :

CEDi		FPDj		Output	
number	Comment	number	Comment	number	Comment
0		X		0	
x		0		0	
1		1		1	coinc ij
1		2	a et b	2	M12Fa et M12Fb
2	a et b	1		2	M12Ca et M12Cb
1		14	2 min , 14 Max	14	M22F[13..0]
9	2 min , 9 Max	1		9	M22C[8..0]
9	**2 min , 9 Max**	**14**	**2 min , 14 Max**	**23**	**M12F[13..0] et M22C[8..0]**

This combination represent 9,54 % (23/241) of the total cell number used by the design => **TOG_{LC} : 9,54%**

7.1.1.3. Definition of the core component power

Iccint = (0,71 x 241) + (0,30 x (512 – 241)) + (0,014 x 241 x 83 x 0,0954)
= 171,11 + 81,30 + 26,72
Iccint = 279,13 mA

7.1.2. Power of the integrate circuit pads

The Pio power is function of the output load characteristic, of the switch frequency and the static power of the input/output pads.

Pio = PstatI + PstatO + Pdyn and by extension Iio = IstatI + IstatO + Idyn

For the EPM7000AE family, the static consumption are :

- For an input pad : 10 µA = IstatI
- For an output pad : 32 µA = IstatO

7.1.2.1. Static current calculation

The design has 29 input and 173 output, which correspond to a static consumption of :
5,826 mA (29 * 10 µA + 173 * 32 µA).

Istat = 5,826 mA

7.1.2.2. Dynamic current calculation

The dynamic current calculation is done with the following formula :

$$Idyn = \sum C_N V_N F_N$$

with C_N : load capacitance (8 pF)
V_N : voltage output (3,3 V)
V_N : output frequency

The design have 173 output which work at a maximum frequency of 83 MHz as we have previously calculated. On all the output available only a certain number of them will change their state at a given time (23 maximum)

$$\mathbf{Idyn_{max} = 23 \times 8\ 10^{-12} \times 3,3 \times 83\ 10^{6} = 50,40\ mA}$$

7.1.2.3. Total pad current calculation

Iio = Istat + Idyn = 5,826 + 50,40 = 56,226 mA

7.1.3. Value of the total power

Considering that the core voltage and the pads voltage are the same value (3,3 V), the power consumption is :

P = Vcc x (Iccint + Iio) = 3,3 x (279,13 + 56,226) = 3,3 x 335,36 = 1,107 W

7.2. INPUT circuits Power consumption (ALTERA EPM7128AE) :

The power consumption can be calculated with the following formula :

P = Pint + Pio = Iccint x Vcc + Pio

With Pint = integrate circuit core power consumption
Iccint = integrate circuit core current
Pio = power consumption of the input/output pads

7.2.1. Power consumption of the core component

The value Iccint can be calculate with the following formula :

$$Iccint = (0,71 \times MC_{TON}) + (0,30 \times (MC_{DEV} - MC_{TON})) + (0,014 \times MC_{USED} \times F_{MAX} \times TOG_{LC})$$

With MC_{TON} : Number of macrocell with the « TURBO BIT « option
MC_{DEV} : Number of macrocell into the component
MC_{USED} : Number of macrocell used in the design
F_{MAX} : Clock Frequency used in the design (in MHz)
TOG_{LC} : Percentage of cell changing state at each clock edge (typ. 12,5%)

After definition and simulation of the FPGA content the applicable parameters are :
MC_{TON} : 104
MC_{DEV} : 128
MC_{USED} : 104

7.2.1.1. Maximum frequency definition :

The maximum frequency c an be define as been the invert of the time between the BPO2 signal (sample signal of the outputs) and the BPO1 signal (reset signal of the output flip flops) :

$$T = 12 \text{ nS} \Rightarrow F_{MAX} = (1/12) * 10^{-9} = \mathbf{83 \text{ MHz} = F_{MAX}}$$

7.2.1.2. Maximum number of cell which change state on the BPO2 signal rising edge :

The maximum number of cell which change of state at a given time can been define as the number of cell changing state when all the CED and FPD detector are active at the front active of the sampled signal BPO2.
There is 23 flip flop which correspond to this characteristic, it is the « CONDITIONNED DIRECT » flip flop (Cci et CFj).

This combination represent 22,12 % (23/104)) of the total cell number used by the design => **TOG_{LC} : 22,12%**

7.2.1.3. Definition of the core component power

Iccint = (0,71 x 104) + (0,30 x (128 – 104)) + (0,014 x 104 x 83 x 0,2212)
= 73,84 + 7,20 + 26,73
Iccint = 107,77 mA

7.2.2. Power of the integrate circuit pads

The Pio power is function of the output load characteristic, of the switch frequency and the static power of the input/output pads.

Pio = PstatI + PstatO + Pdyn and by extension Iio = IstatI + IstatO + Idyn

For the EPM7000AE family, the static consumption are :

- For an input pad : 10 µA = IstatI

- For an output pad : 32 µA = IstatO

7.2.2.1. Static current calculation

The design has 31 input and 49 output, which correspond to a static consumption of :
1,878 mA (31 * 10 µA + 49 * 32 µA).

Istat = 1,878 mA

7.2.2.2. Dynamic current calculation

The dynamic current calculation is done with the following formula :

$$Idyn = \sum C_N V_N F_N$$

with C_N : load capacitance (8 pF)
V_N : voltage output (3,3 V)
V_N : output frequency

The design have 49 output which work at a maximum frequency of 83 MHz as we have previously calculated. On all the output available only a certain number of them will change their state at a given time (23 maximum)

$$\mathbf{Idyn_{max} = 23 \times 8\ 10^{-12} \times 3,3 \times 83\ 10^{6} = 50,40\ mA}$$

7.2.2.3. Total pad current calculation

Iio= Istat + Idyn = 1,878 + 50,40 = 52,278 mA

7.2.3. Value of the total power

Considering that the core voltage and the pads voltage are the same value (3,3 V), the power consumption is :

P = Vcc x (Iccint + Iio) = 3,3 x (107,77 + 52,278) = 3,3 x 160,05 = 0,53 W

7.3. Calculation of the necessary power for the component powered under 3,3 V

Considering that the component supply voltage is done through a voltage regulator based to the +5V supply voltage, the power supply, under the +5V power supply, will be like below :

	Octant 0			Octant 1			Total	Units
	CEDPD20	INPUT	Regulator	CEDPD20	INPUT	Regulator		
I_{totale}	335,36	160,05	495,41	335,36	160,05	495,41	990,82	mA
U_{alim}	3,3	3,3	5 – 3,3 = 1,7	3,3	3,3	5 – 3,3 = 1,7	5	V
$P_{dissipée}$	1107	528	842,197	1107	528	842,197	4954,10	mW

7.4. CEDFPD VXI circuits Power consumption (ALTERA EPM7128S) :

The power consumption can be calculated with the following formula :

$$P = Pint + Pio = Iccint \times Vcc + Pio$$

With Pint = integrate circuit core power consumption
Iccint = integrate circuit core current
Pio = power consumption of the input/output pads

7.4.1. Power consumption of the core component

The value Iccint can be calculate with the following formula :

$$Iccint = (0,93 \times MC_{TON}) + (0,40 \times (MC_{DEV} - MC_{TON})) + (0,040 \times MC_{USED} \times F_{MAX} \times TOG_{LC})$$

With
MC_{TON} : Number of macrocell with the « TURBO BIT « option
MC_{DEV} : Number of macrocell into the component
MC_{USED} : Number of macrocell used in the design
F_{MAX} : Clock Frequency used in the design (in MHz)
TOG_{LC} : Percentage of cell changing state at each clock edge (typ. 12,5%)

After definition and simulation of the FPGA content the applicable parameters are :
MC_{TON} : 115
MC_{DEV} : 128
MC_{USED} : 115
F_{MAX} : 16 (MHz)
TOG_{LC} : 0,125

Iccint = (0,93 x 115) + (0,40 x (128 – 115)) + (0,040 x 115 x 16 x 0,125)
= 106,95 + 5,2 + 9,20
Iccint = 121,35 mA

7.4.2. Power of the integrate circuit pads

The Pio power is function of the output load characteristic, of the switch frequency and the static power of the input/output pads.

Pio = PstatI + PstatO + Pdyn and by extension Iio = IstatI + IstatO + Idyn

For the EPM7000S family, the static consumption are :
- For an input pad : 10 µA = IstatI
- For an output pad : 32 µA = IstatO

7.4.2.1. Static current calculation

The design have :
- 22 input
- 42 output
- 16 input/output.

Which correspond to a static consumption of :

Istat = 22 * 10 µA + 42 * 32 µA + 16 * 32 µA **= 2,076 mA = Istat**

7.4.2.2. Dynamic current calculation

The dynamic current calculation is done with the following formula :

$$Idyn = \sum C_N V_N F_N$$

with C_N : load capacitance (10 pF)
V_N : voltage output (3,3 V)
V_N : output frequency

The design have 41 output and on all the output available only a certain number of them will change their state at a given time.
The maximum number of cell changing their state at a given time is 17 :

- Write into the ETAT register(10)
- Delayed output of the write signal (1)
- DATA_ACKNOWLEDGE output (1)
- /FORCEINT output (1)
- Output control for the COUNT32 components (5) : INHIB_C, INHIB_NC, LO, RST_CPT

For an easiest calculation, the output signal frequency will be equal to the faster output signal frequency that is to say 8 MHz.

Idyn = 17 * 10 10^{-12} * 5 * 8 10^{6} = 6,8 mA = Idyn

7.4.2.3. Total pad current calculation

Iio = IstatI + IstatO + Idyn = 2,076 + 6,8 **= 8,876 mA = Iio**

7.4.3. Value of the total power

P = Pint + Pio = Iccint x Vcc + Iio x Vcc
P = 5 x (121,35 + 8,876) = 5 x 130,226
P = 651,13 mW

7.5. Power calculation for the fast hardware (ECL)

The typical and maximum power consumption of the different component in ECL technology is given below as well as the calculated value of the total typical consumption and the total maximum consumption of the negative power supply (necessary for the definition of the power supply fuse).
The current are all given in mA and when the typical in not known, the maximum value is used.

Components	Current under + 5V		Current under – 5V		Number	Total current under + 5V		Total current under – 5V	
	typical	max	typical	max		typical	max	Typical	max
MC 10 EL 31			27	32	50			1350	1600
MC 10 H 101			20	29	7			140	203
MC 10 115			22	29	12			264	348
MC 10 H 124	25	25	72	72	3	75	75	216	216
MC 10 H 125	63	63	44	44	25	1575	1575	1100	1100
MC 10 164			62	83	1			62	83
MC 10 192			115	154	2			230	308
AD 8561	7,5	7,5	5,5	5,5	3	22,5	22,5	16,5	16,5
MAX 9690	0	0	0	0	2	0	0	0	0
					Total :	1672,5	1672,5	**3527**	**3874,5**

7.6. Power calculation for the hardware under (TTL)

The typical and maximum power consumption of the different component in TTL technology is given below as well as the calculated value of the total typical consumption and the total maximum consumption of the negative power supply (necessary for the definition of the power supply fuse).
The current are all given in mA and when the typical in not known, the maximum value is used.

Components	Typical current under + 5V	Maximum current under + 5V	Number	Total typical current under + 5V	Total maximum current under + 5V
Trans. ECL	1672,5	1672,5	1	1 672,50	1 672,50
ALTERA 3,3 V	495,41	495,41	2	990,82	990,82
CEDFPDVXI	130,226	130,226	1	130,23	130,23
COMPTEUR32	30	30	17	510,00	510,00
IT 9010	80	80	1	80,00	80,00
DS 1020	30	30	1	30,00	30,00
MAX 811	0,006	0,015	2	0,01	0,03
74 LS 14	38	60	1	38,00	60,00
74 F 138	13	20	2	26,00	40,00
74 F 245	95	120	10	950,00	1 200,00
74 FCT 245	3,5	6,5	12	42,00	78,00
PALCE 16V8	55	55	1	55,00	55,00
LED 3 mm	10	10	2	20,00	20,00
			Total board :	**4 544,56**	**4 866,58**

7.7. Power calculation for the –2V voltage

The output voltage characteristic of the different component in ECL technology are given below to permit the calculation of the –2V power supply absorbed current.
Among the characteristics of them it has been used only the value of the worst case.

		Min	max	Unit	Temp.
10 EL 31	Output High	- 1,025	**- 0,880**	V	85 °C
	Output Low	- 1,810	-1,620	V	85 °C
MAX 9690	Output High	- 0,92	- 0,735	V	75 °C
	Output Low	- 1,95	- 1,6	V	75 °C
MC 10 H 101	Output High	- 0,92	- 0,735	V	75 °C
	Output Low	- 1,95	- 1,6	V	75 °C
MC 10 H 115	Output High	- 0,92	- 0,735	V	75 °C
	Output Low	- 1,95	- 1,6	V	75 °C
MC 10 H 124	Output High	- 0,92	**- 0,735**	V	75 °C
	Output Low	- 1,95	- 1,6	V	75 °C
MC 10 164	Output High	- 0,92	- 0,735	V	75 °C
	Output Low	- 1,95	- 1,6	V	75 °C

The worst case characteristics are marked in bold.

Component	number of resistor	Vout (V)	Resistor value	current (A)
10 EL 31	51	0,880	100	0,571
MAX 9690	2	0,735	100	0,025
MC 10 H 101	28	0,735	100	0,354
MC 10 H 115	46	0,735	100	0,582
MC 10 H 124	9	0,735	100	0,114
MC 10 164	1	0,735	100	0,013
			Total :	**1,659**

7.8. Definition of the maximum available intensity

The “observation B.8.1” of the VXI specification rev 1.4 define the current maximum per pin connector.

Observation B.8.1 :
A 1 ampere per pin limit allows the VMEbus rated connector to operate at 55°ambient.

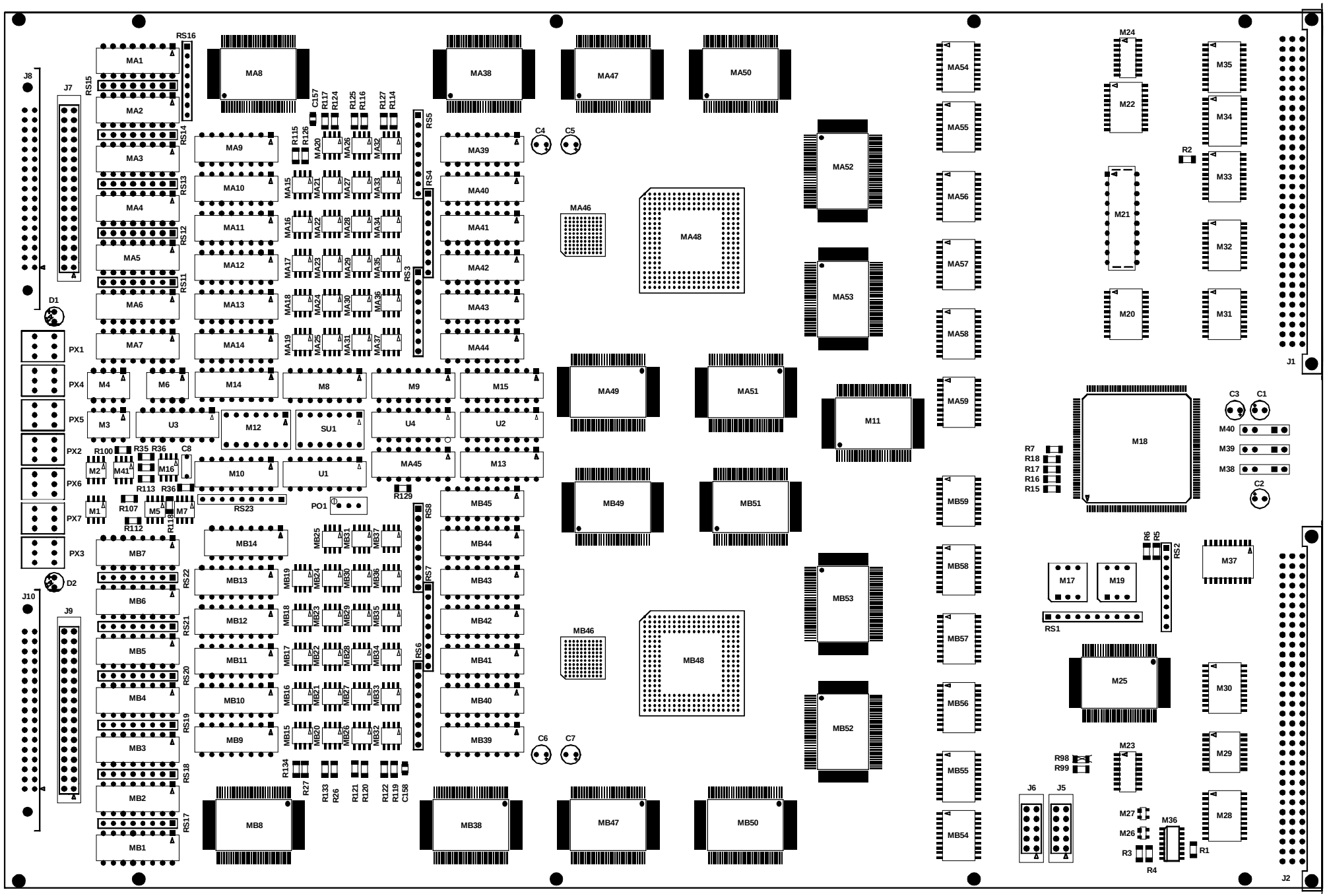
The table below give the maximum current for a board placed in a VXI crate size C.

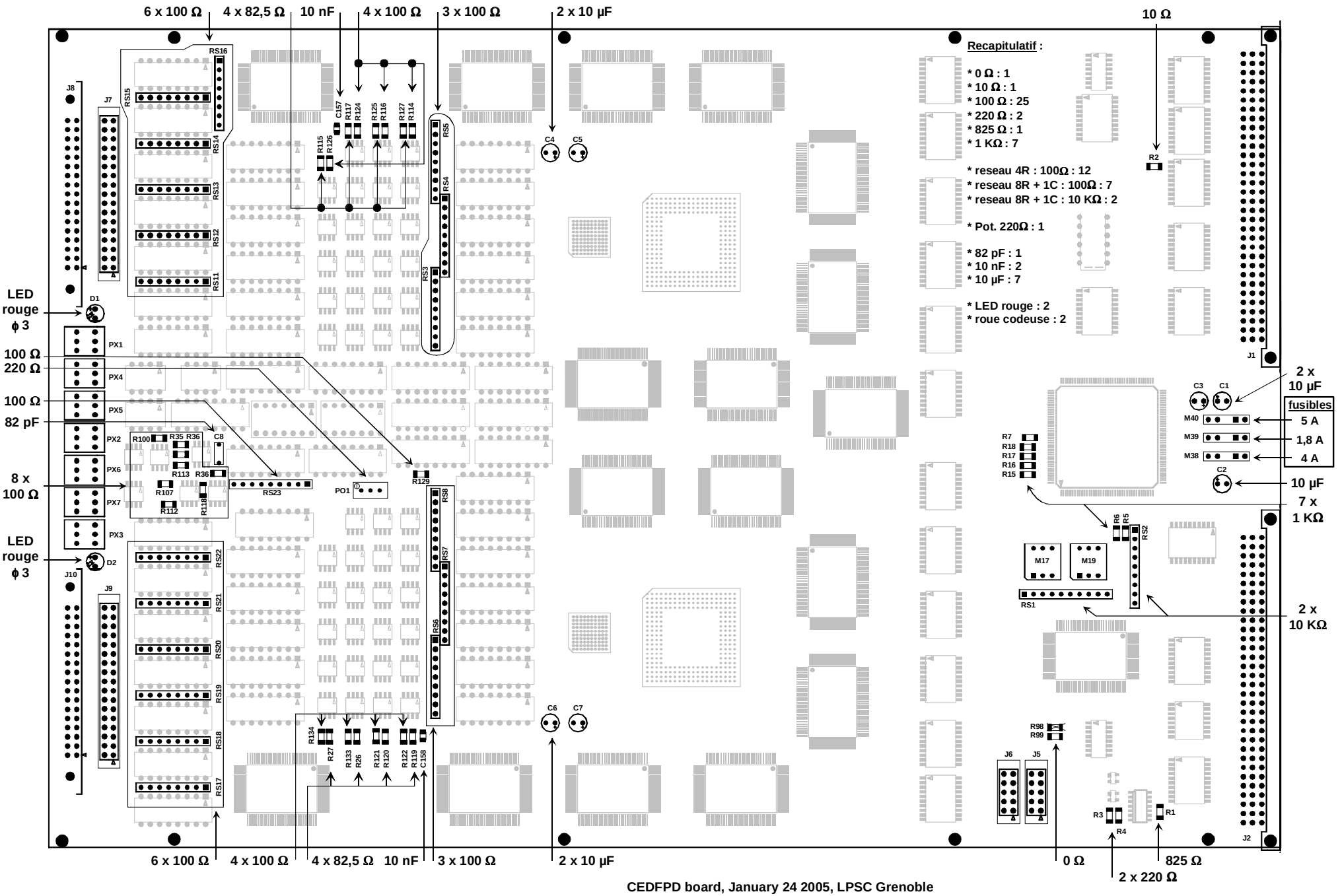
Voltage	Pin number	Imax	Pmax
+ VCC (+ 5 v)	7	7 A	35 W
- VEE (- 5,2 v)	5	5 A	26 W
- VDD (- 2 v)	2	2 A	4 W

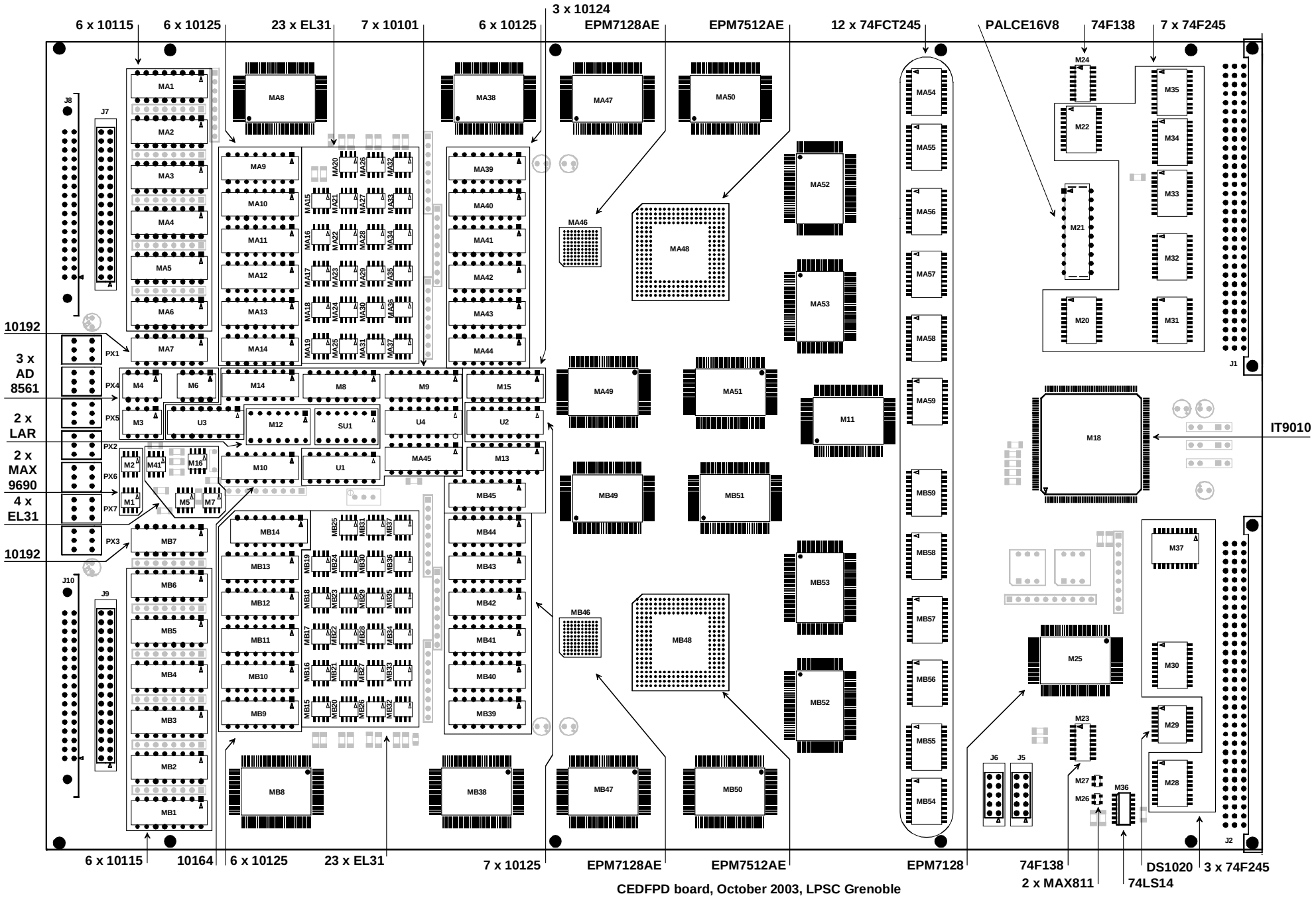
8. Boards assembly

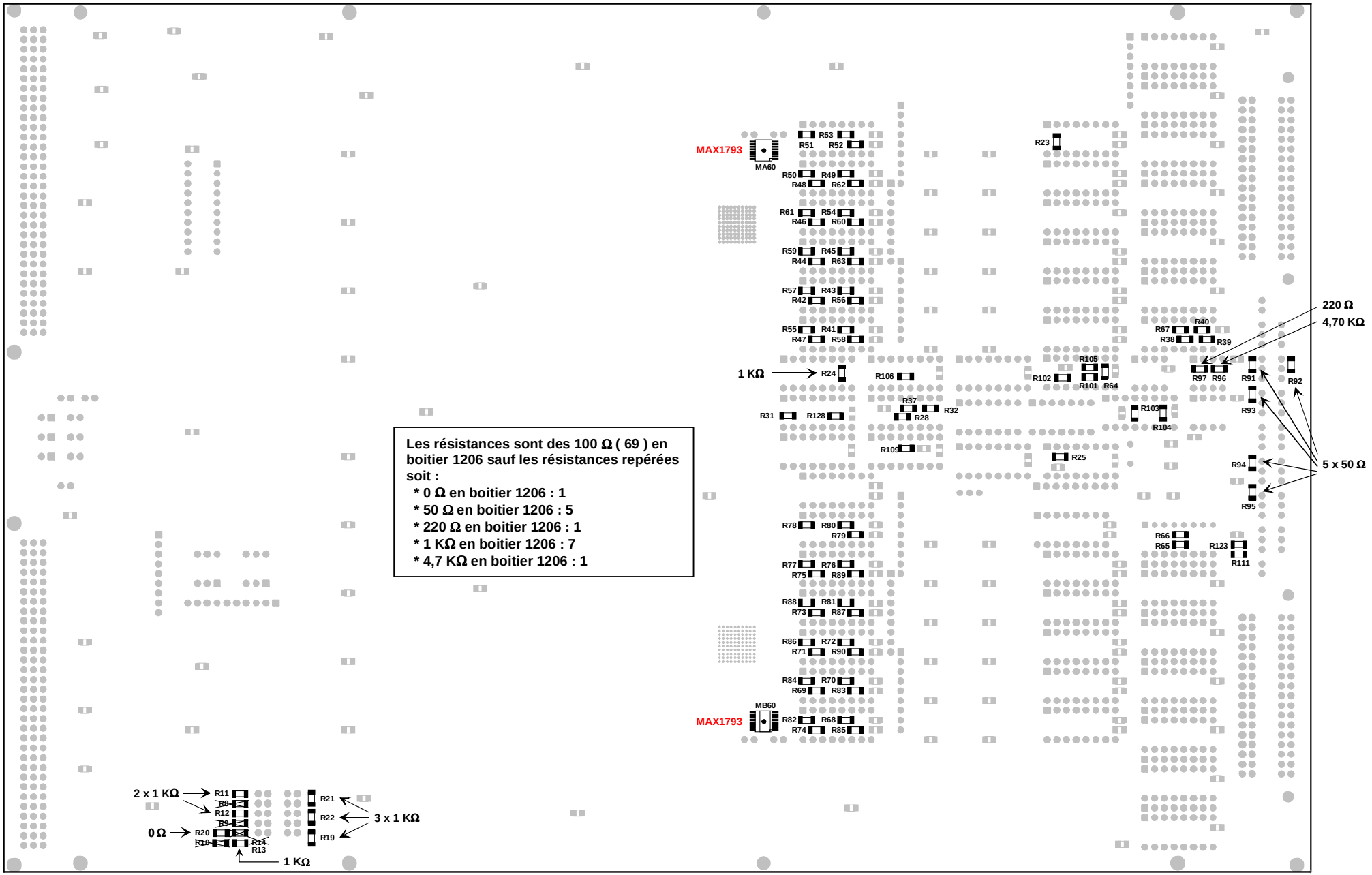
The following picture show where are mounted the different components (passive and active) on the two boards : CEDFPD and CEDFPD_carte_fille.

8.1. CEDFPD board assembly


J8
J7
RS15
RS16
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
RS14
RS13
RS12
RS11
D1
PX1
PX4
PX5
PX2
PX6
PX7
PX3
D2
J10
J9
M4
M6
M3
U3
M2
M41
M16
M1
M5
M7
R100
R35
R36
C8
R113
R107
R112
RS23
M14
M12
SU1
M10
U1
M8
M9
M15
U4
U2
MA45
M13
R129
PO1
MA9
MA10
MA11
MA12
MA13
MA14
MA15
MA16
MA17
MA18
MA19
MA20
MA21
MA22
MA23
MA24
MA25
MA26
MA27
MA28
MA29
MA30
MA31
R115
R126
C157
R117
R124
R125
R116
R127
R114
RS5
RS4
RS3
MA38
MA39
MA40
MA41
MA42
MA43
MA44
MA47
MA50
C4
C5
MA46
MA48
MA52
MA53
MA49
MA51
M11
MB14
MB13
MB12
MB11
MB10
MB9
MB8
MB7
MB6
MB5
MB4
MB3
MB2
MB1
RS22
RS21
RS20
RS19
RS18
RS17
MB25
MB19
MB24
MB18
MB23
MB17
MB22
MB16
MB21
MB15
MB20
MB26
MB27
MB28
MB29
MB30
MB31
MB32
MB33
MB34
MB35
MB36
MB37
R134
R27
R133
R26
R121
R120
R122
R119
C158
RS8
RS7
RS6
MB45
MB44
MB43
MB42
MB41
MB40
MB39
MB38
MB47
MB50
C6
C7
MB46
MB48
MB52
MB49
MB51
MB53
MA54
MA55
MA56
MA57
MA58
MA59
MB59
MB58
MB57
MB56
MB55
MB54
M24
M22
M21
M20
M35
M34
M33
M32
M31
J1
R2
M18
C3
C1
M40
M39
M38
C2
R7
R18
R17
R16
R15
R6
R5
RS2
M37
M17
M19
RS1
M25
M30
M29
M28
M23
R98
R99
J6
J5
M27
M26
R3
R4
M36
R1
J2

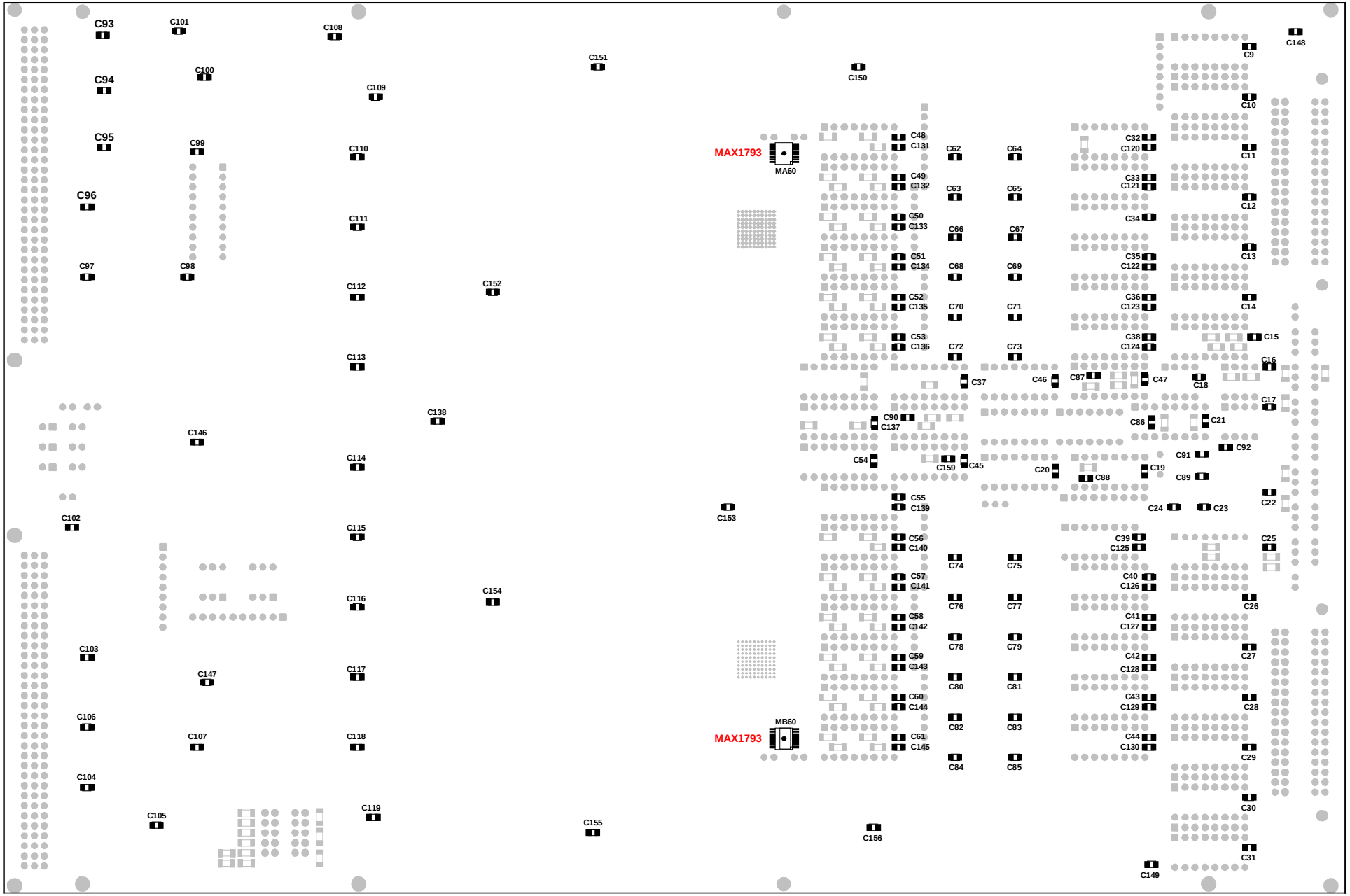

6 x 100 Ω
4 x 82,5 Ω
10 nF
4 x 100 Ω
3 x 100 Ω
2 x 10 µF
10 Ω
Recapitulatif :
* 0 Ω : 1
* 10 Ω : 1
* 100 Ω : 25
* 220 Ω : 2
* 825 Ω : 1
* 1 KΩ : 7
* reseau 4R : 100Ω : 12
* reseau 8R + 1C : 100Ω : 7
* reseau 8R + 1C : 10 KΩ : 2
* Pot. 220Ω : 1
* 82 pF : 1
* 10 nF : 2
* 10 µF : 7
* LED rouge : 2
* roue codeuse : 2
LED rouge ϕ 3
100 Ω
220 Ω
100 Ω
82 pF
8 x 100 Ω
LED rouge ϕ 3
2 x 10 µF
fusibles
5 A
1,8 A
4 A
10 µF
7 x 1 KΩ
2 x 10 KΩ
0 Ω
825 Ω
2 x 220 Ω
CEDFPD board, January 24 2005, LPSC Grenoble


6 x 10115
6 x 10125
23 x EL31
7 x 10101
6 x 10125
3 x 10124
EPM7128AE
EPM7512AE
12 x 74FCT245
PALCE16V8
74F138
7 x 74F245
10192
3 x AD 8561
2 x LAR
2 x MAX 9690
4 x EL31
10192
IT9010
6 x 10115
10164
6 x 10125
23 x EL31
7 x 10125
EPM7128AE
EPM7512AE
EPM7128
74F138
2 x MAX811
74LS14
DS1020
3 x 74F245
CEDFPD board, October 2003, LPSC Grenoble



Carte CEDFPD, Octobre 2003, LPSC Grenoble

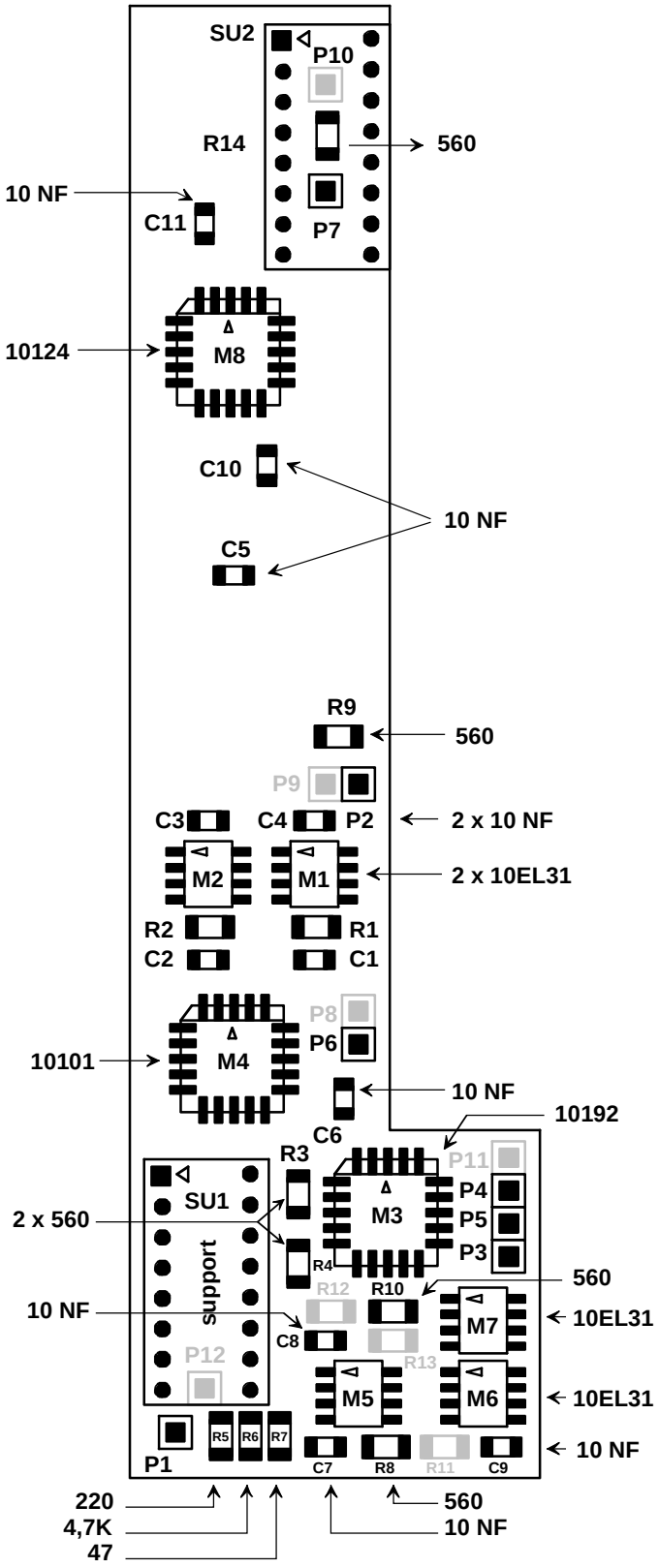
Toutes les capacités (149) sont des 10 NF en boitier 0805



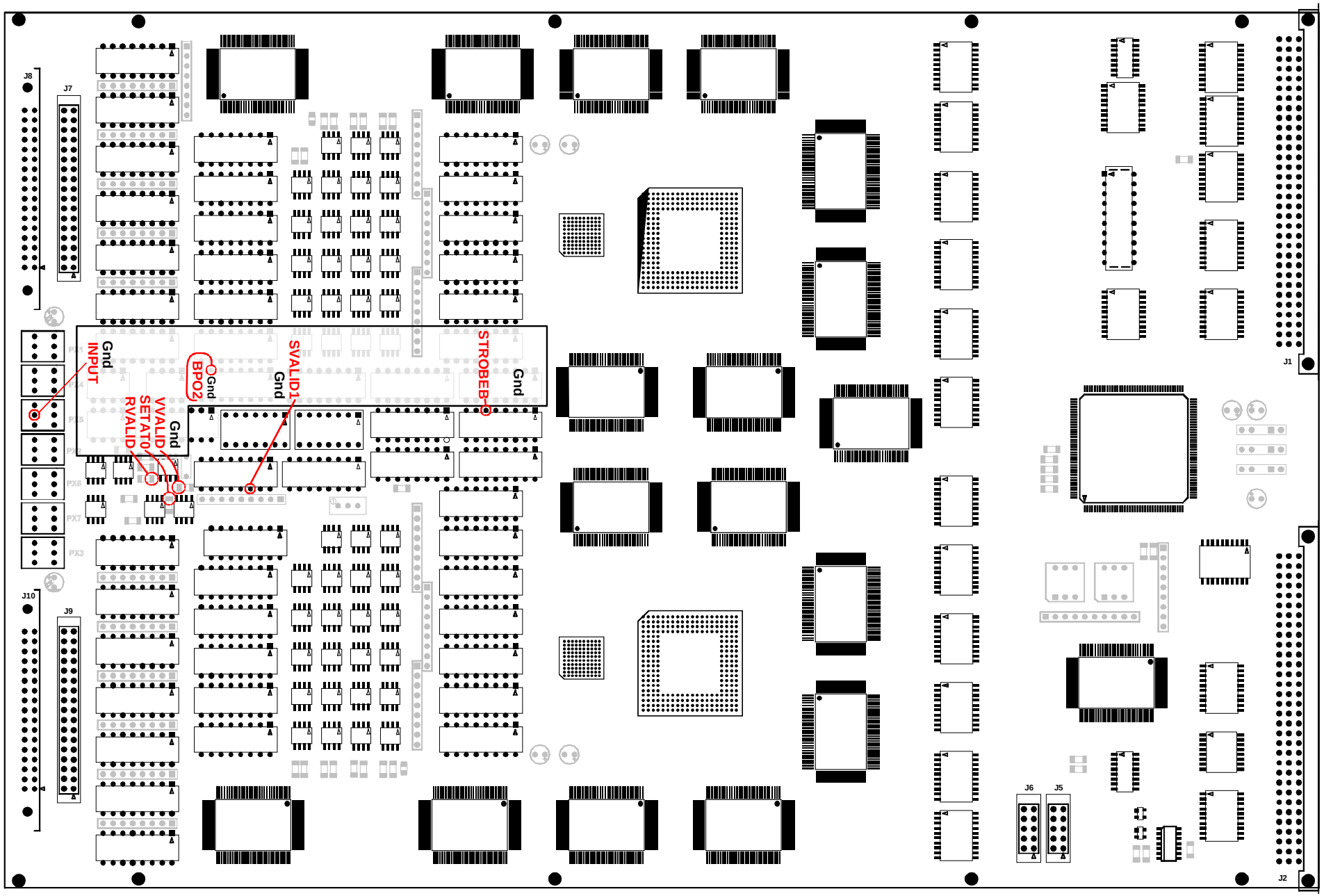
Carte CEDFPD, Octobre 2003, LPSC Grenoble

8.2. CEDFPD_carte_fille board assembly

8.2.1. Components view

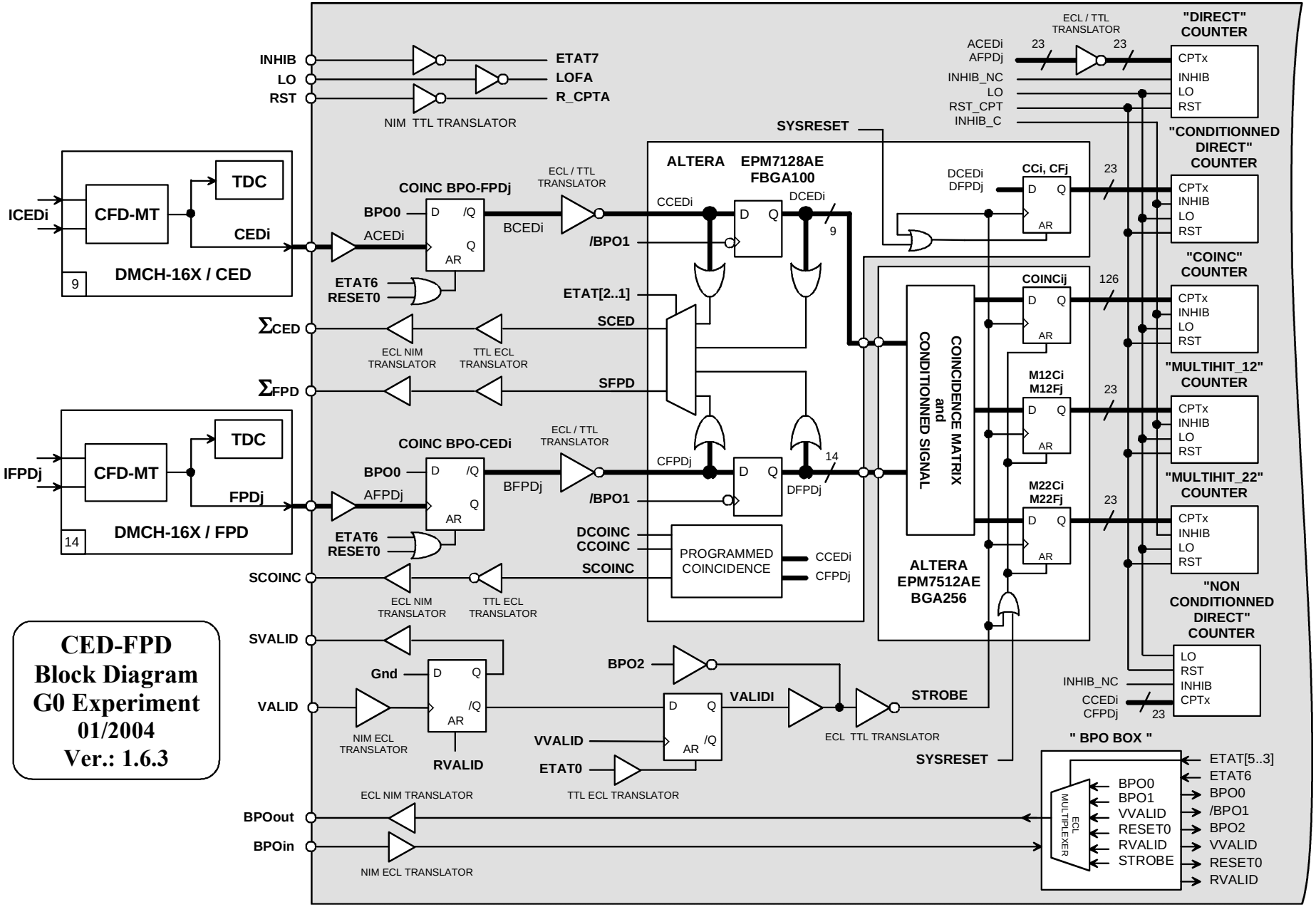


8.2.2. View of the CEDFPD and CEDFPD_carte_fille boards assembly

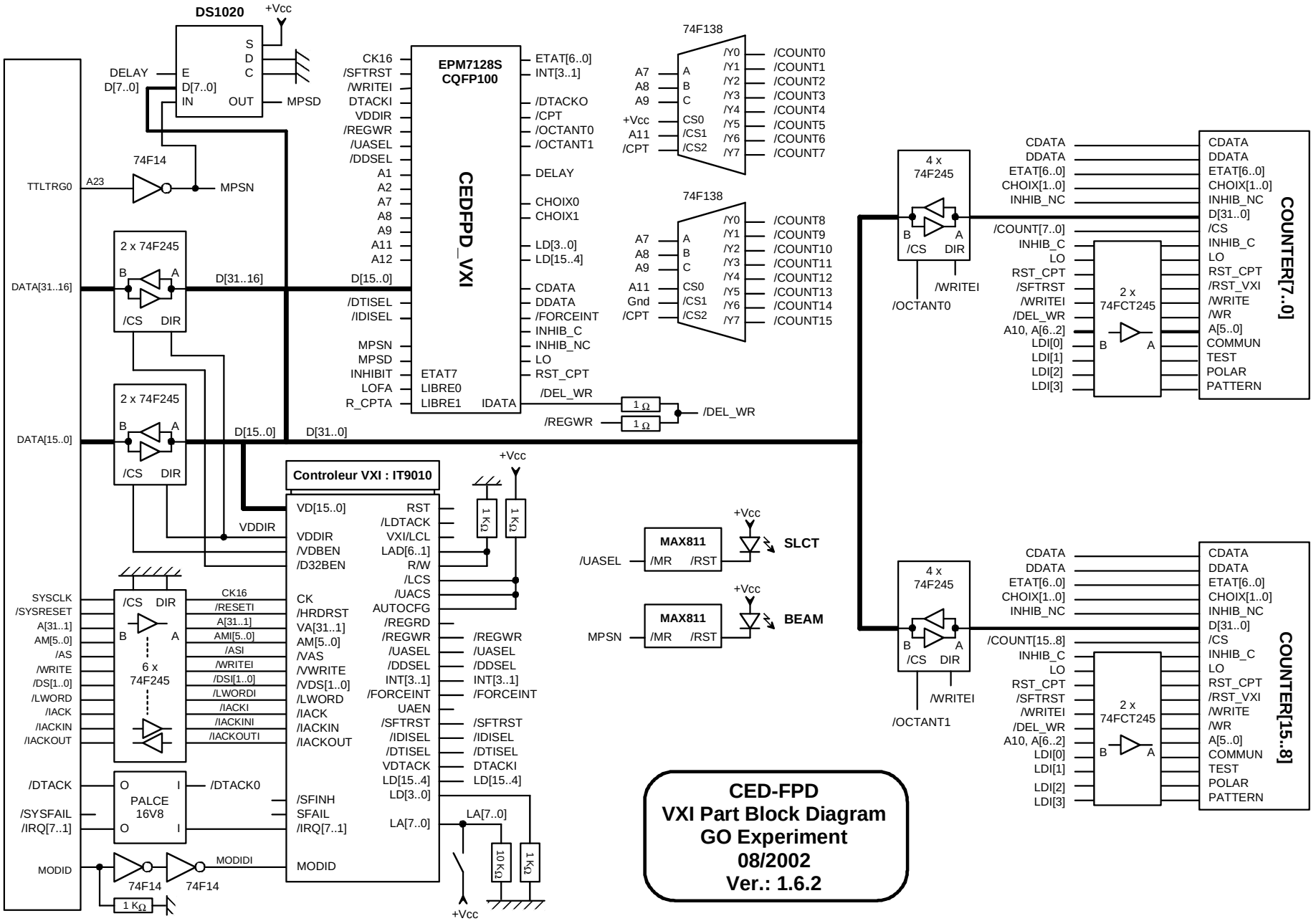


CEDFPD board, October 2004, LPSC Grenoble

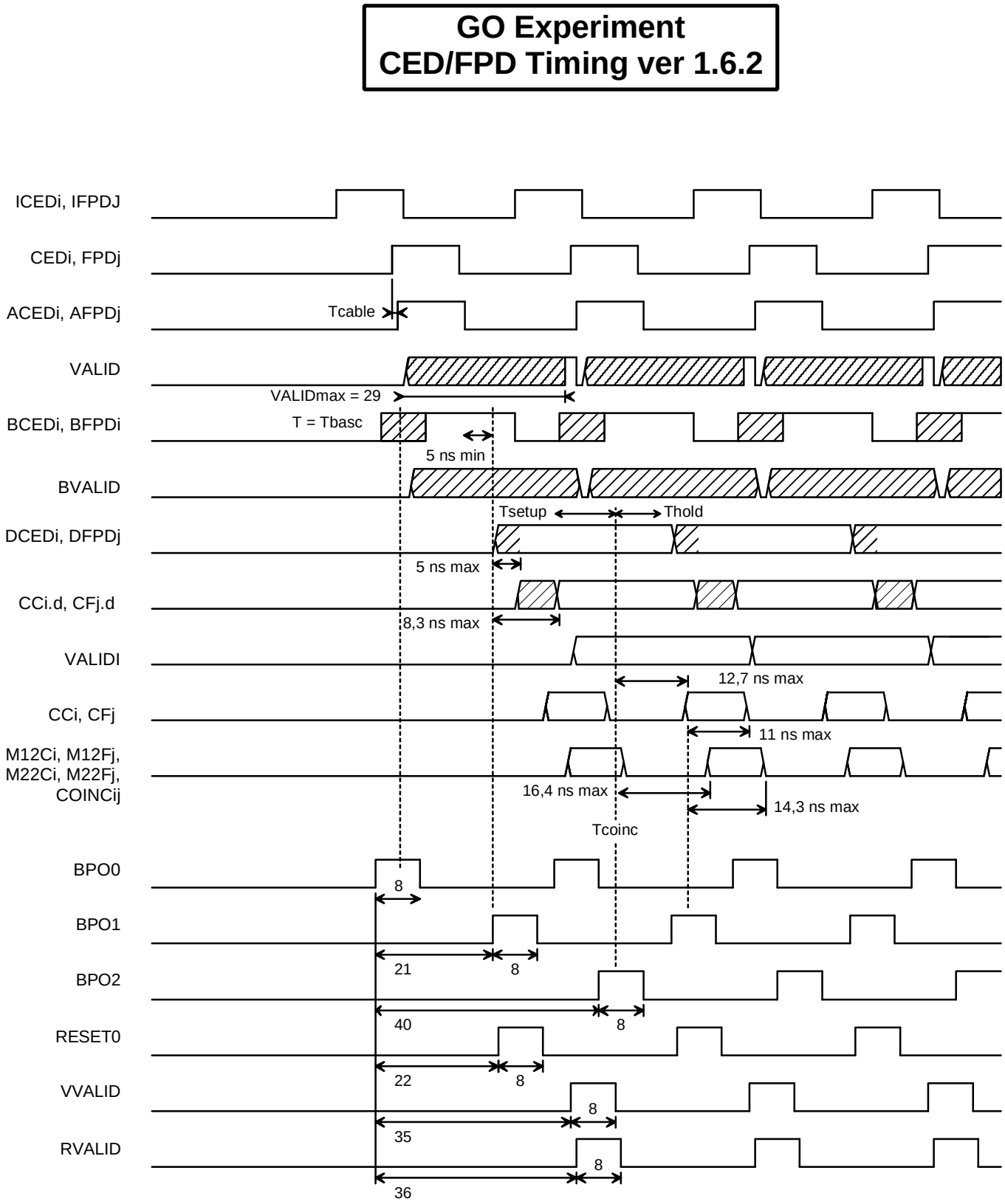
Annex 1 : Front end Synoptic



Annex 2 : Back End Synoptic



Annex 3 : Timing of the control signals



Annex 4 : Pin out of the CED/FPD input connector

Tableau 1 : pin out of the CED input connector

Name	N°	N°	Name
CED0 (diff. Positive)	1	2	CED0 (diff. negative)
CED1 (diff. Positive)	3	4	CED1 (diff. negative)
CED2 (diff. Positive)	5	6	CED2 (diff. negative)
CED3 (diff. Positive)	7	8	CED3 (diff. negative)
CED4 (diff. Positive)	9	10	CED4 (diff. negative)
CED5 (diff. Positive)	11	12	CED5 (diff. negative)
CED6 (diff. Positive)	13	14	CED6 (diff. negative)
CED7 (diff. Positive)	15	16	CED7 (diff. negative)
CED8 (diff. Positive)	17	18	CED8 (diff. negative)
N.C.	19	20	N.C.
N.C.	21	22	N.C.
N.C.	23	24	N.C.
N.C.	25	26	N.C.
N.C.	27	28	N.C.
N.C.	29	30	N.C.
N.C.	31	32	N.C.
GND	33	34	GND

Tableau 2 : pin out of the FPD input connector

Name	N°	N°	Name
FPD0 (diff. Positive)	1	2	FPD0 (diff. negative)
FPD1 (diff. Positive)	3	4	FPD1 (diff. negative)
FPD2 (diff. Positive)	5	6	FPD2 (diff. negative)
FPD3 (diff. Positive)	7	8	FPD3 (diff. negative)
FPD4 (diff. Positive)	9	10	FPD4 (diff. negative)
FPD5 (diff. Positive)	11	12	FPD5 (diff. negative)
FPD6 (diff. Positive)	13	14	FPD6 (diff. negative)
FPD7 (diff. Positive)	15	16	FPD7 (diff. negative)
FPD8 (diff. Positive)	17	18	FPD8 (diff. negative)
FPD9 (diff. Positive)	19	20	FPD9 (diff. negative)
FPD10 (diff. Positive)	21	22	FPD10 (diff. negative)
FPD11 (diff. Positive)	23	24	FPD11 (diff. negative)
FPD12 (diff. Positive)	25	26	FPD12 (diff. negative)
FPD13 (diff. Positive)	27	28	FPD13 (diff. negative)
N.C.	29	30	N.C.
N.C.	31	32	N.C.
GND	33	34	GND

Annex 5 : Pin out of the VXI connector

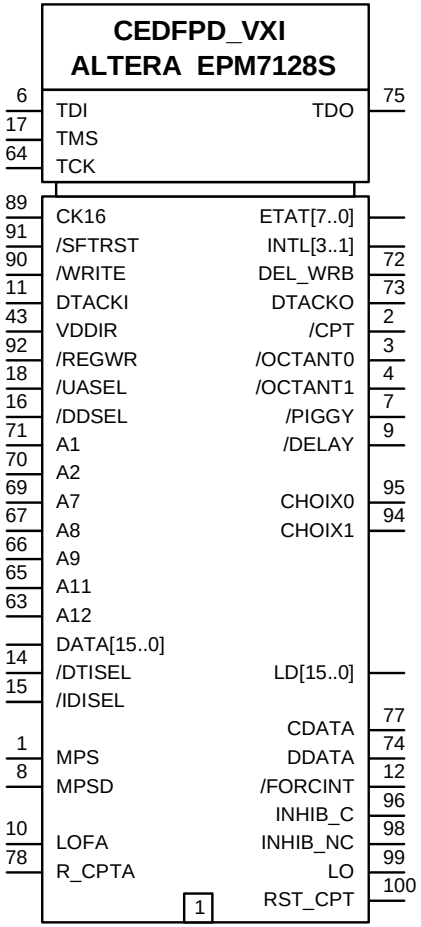
P1 Connector

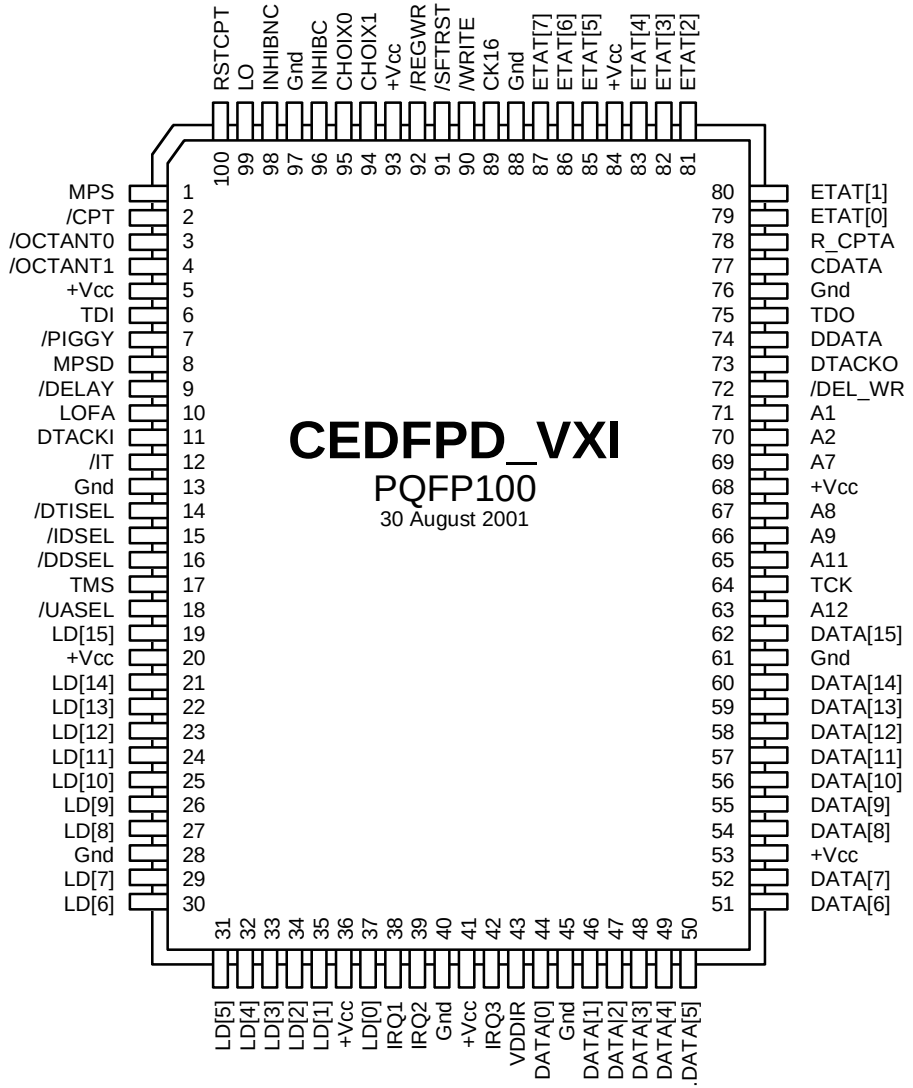
N°	Row A	Row B	Row C
1	D00	/BBUSY	D08
2	D01	/BCLR	D09
3	D02	/ACFAIL	D10
4	D03	/BG0IN	D11
5	D04	/BG0OUT	D12
6	D05	/BG1IN	D13
7	D06	/BG1OUT	D14
8	D07	/BG2IN	D15
9	GND	/BG2OUT	GND
10	SYSCLK	/BG3IN	/SYSFAIL
11	GND	/BG3OUT	/BERR
12	/DS1	/BR0	/SYSRESET
13	/DS0	/BR1	/LWORD
14	/WRITE	/BR2	AM5
15	GND	/BR3	A23
16	/DTACK	AM0	A22
17	GND	AM1	A21
18	/AS	AM2	A20
19	GND	AM3	A19
20	/IACK	GND	A18
21	/IACKIN	SERCLK	A17
22	/IACKOUT	SERDAT	A16
23	AM4	GND	A15
24	A07	/IRQ7	A14
25	A06	/IRQ6	A13
26	A05	/IRQ5	A12
27	A04	/IRQ4	A11
28	A03	/IRQ3	A10
29	A02	/IRQ2	A09
30	A01	/IRQ1	A08
31	- 12	+ 5 v STDBY	+ 12 v
32	+ 5 v	+ 5 v	+ 5 v

P2 Connector

N°	Row A	Row B	Row C
1	HF	+ 5 v	CLK10+
2	- 2 V	Gnd	CLK10-
3	/HF	Reserved	Gnd
4	Gnd	A[24]	- 5,2 V
5		A[25]	
6		A[26]	
7	- 5,2 V	A[27]	Gnd
8		A[28]	
9		A[29]	
10	Gnd	A[30]	Gnd
11		A[31]	
12		Gnd	
13	- 5,2 V	+ 5 v	- 2 V
14		D[16]	
15		D[17]	
16	Gnd	D[18]	Gnd
17		D[19]	
18	HELin (local bus 09)	D[20]	HELout (local bus 09)
19	- 5,2 V	D[21]	- 5,2 V
20	QRTin (local bus 10)	D[22]	QRTout (local bus 10)
21	Localin (local bus 11)	D[23]	Localout (local bus 11)
22	Gnd	GND	Gnd
23	/MPS	D[24]	120H0
24	120H1	D[25]	T120
25	+ 5 V	D[26]	Gnd
26	/MRUN	D[27]	DHF
27	/MRST*	D[28]	LTPO
28	Gnd	D[29]	Gnd
29		D[30]	
30	MODID	D[31]	Gnd
31	Gnd	GND	+ 24 V
32	TST	+ 5 v	- 24 V

Annex 6 : CEDFPD_VXI Component





Gnd : 13, 28, 40, 45, 61, 76, 88, 97

+Vcc : 5, 20, 36, 41, 53, 68, 84, 93

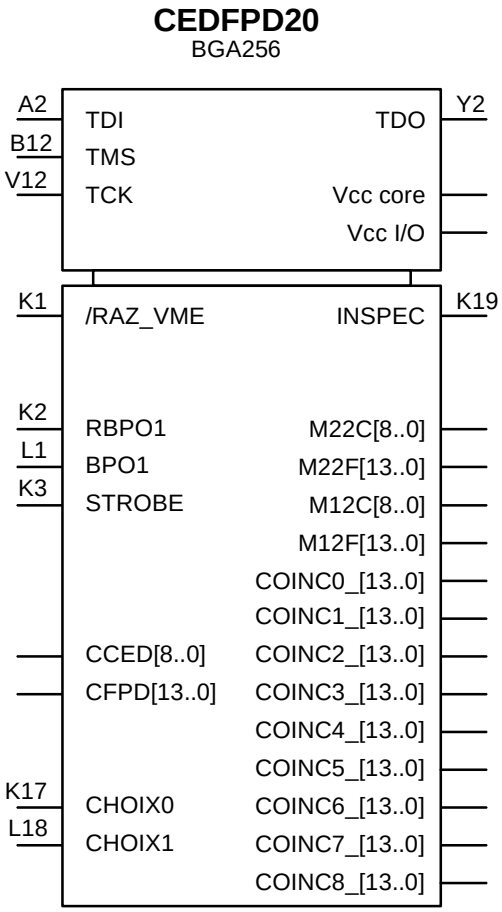
LD[15..0] : 37, 35, 34, 33, 32, 31, 30, 29, 27, 26, 25, 24, 23, 22, 21, 19

INTL[3..1] : 38, 39, 42

DATA[15..0] : 44, 46, 47, 48, 49, 50, 51, 52, 54, 55, 56, 57, 58, 59, 60, 62

ETAT[7..0] : 79, 80, 81, 82, 83, 85, 86, 87

Annex 7 : Body of the CEDFPD20 component



CCED[8..0] : P3, P2, P1, N4, N3, N2, N1, M4, M3

CFPD[13..0] : M2, M1, L3, J4, J3, J2, H4, H3, H2, H1, G4, G3, G2, G1

M22C[8..0] : D7, C7, B7, A7, D8, C8, B8, A8, D9,

M22F[13..0] : C9, B9, A9, D10, C10, B10, A10, D11, C11, B11, A11, D12, C12, A12,

M12C[8..0] : F4, F3, F2, F1, E3, E2, E1, D2, D1,

M12F[13..0] : C2, C1, B1, B3, A3, B4, A4, C5, B5, A5, D6, C6, B6, A6,

COINC0_[13..0] : D13, C13, B13, A13, D14, C14, B14, A14, D15, C15, B15, A15, C16, B16,

COINC1_[13..0] : A16, B17, A17, B18, A18, A19, A20, C19, C20, D19, D20, E18, E19, E20,

COINC2_[13..0] : F17, F18, F19, F20, G17, G18, G19, G20, H17, H18, H19, H20, J17, J18,

COINC3_[13..0] : K20, L20, M17, M18, N17, N18, N19, N20, P17, P18, P19, P20, R17, R18,

COINC4_[13..0] : R19, R20, T18, T19, T20, U19, U20, V20, W20, Y19, W18, Y18, W17, Y17,

COINC5_[13..0] : V16, W16, Y16, U15, V15, W15, Y15, U14, V14, W14, Y14, U13, V13, W13,

COINC6_[13..0] : Y13, U12, W12, Y12, U11, V11, W11, Y11, U10, V10, W10, Y10, U9, V9,

COINC7_[13..0] : W9, Y9, U8, V8, W8, Y8, U7, V7, W7, Y7, U6, V6, W6, Y6,

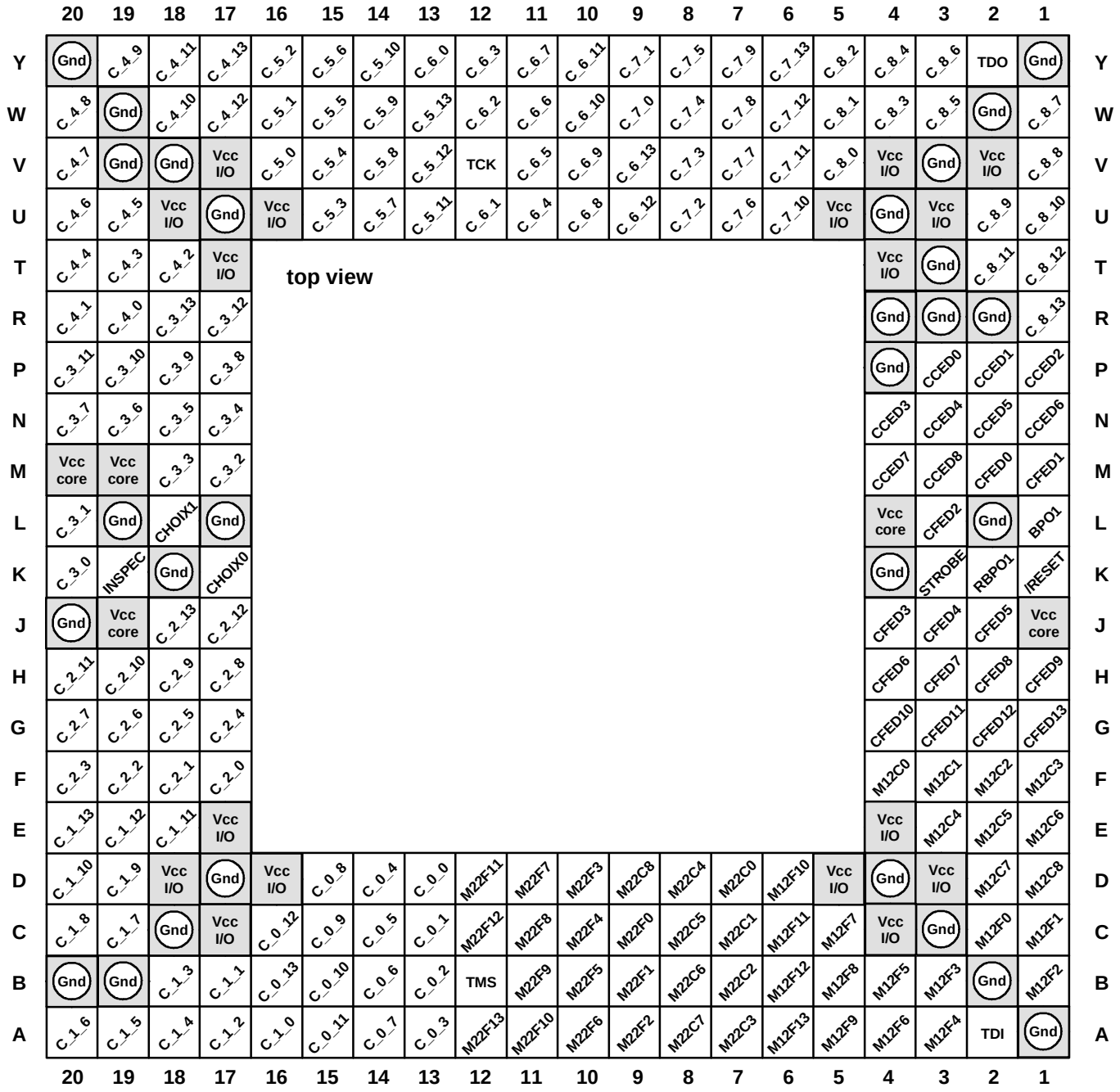
COINC8_[13..0] : V5, W5, Y5, W4, Y4, W3, Y3, W1, V1, U2, U1, T2, T1, R1,

Vcc I/O : C4, C17, D3, D5, D16, D18, E4, E17, T4, T17, U3, U5, U16, U18, V2, V4, V17

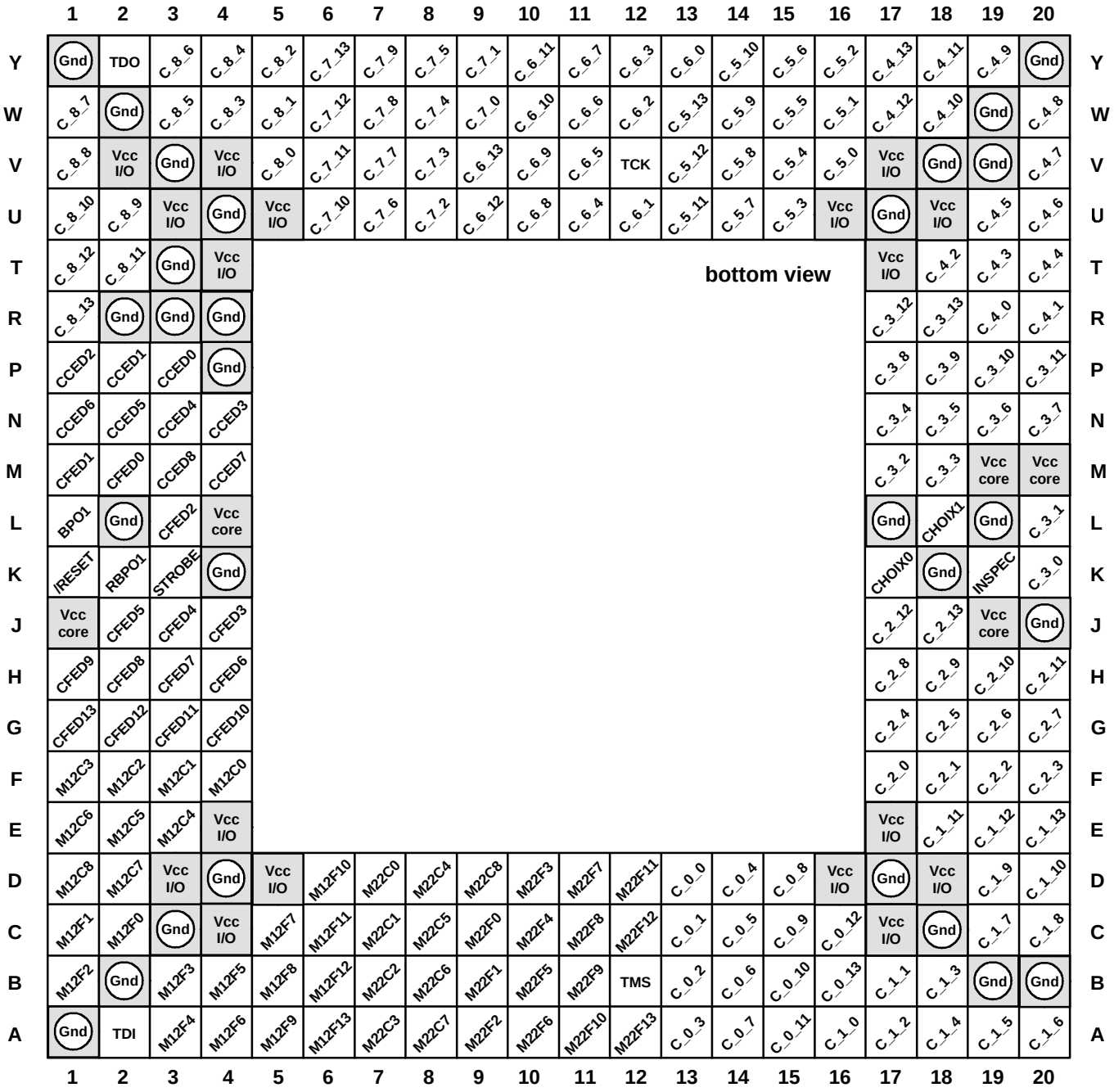
Vcc core : J1, J19, L4, M19, M20

Gnd : A1, B2, B19, B20, C3, C18, D4, D17, J20, K4, K18, L2, L17, U4, U17, V3, V18, V19, W2, W19, Y1, Y20, L19, P4, R4, R3, T3, R2

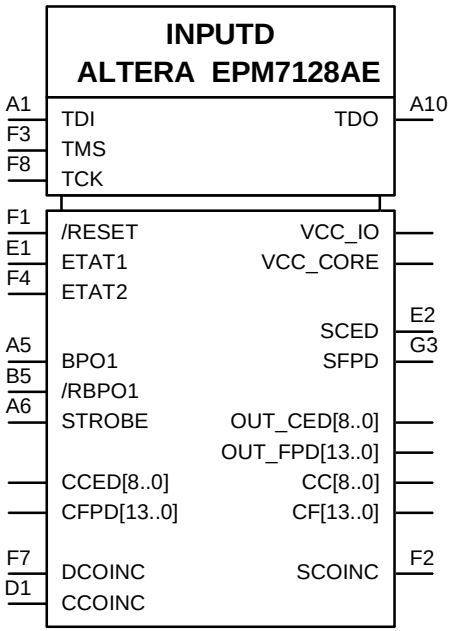
Annex 8 : Pin out of the CEDFPD20 component (top view)



Annex 9 : Pin out of the CEDFPD20 component (bottom view)



Annex 10 : body of the INPUT component



Gnd : C3, D6, D7, E5, F6, G4, G5, H8

VCC_IO : C8, D4, E6, F5, G7, H3

VCC_CORE : D5, G6

CCED[8..0] : C1, B2, D2, B3, E3, B4, E4, B6, A7

CFPD[13..0] : B1, A2, C2, A3, D3, A4, C4, C5, C6, B7, C7, E7, D8, E8

OUT_CED[8..0] : G1, G2, H1, H2, J1, K1, K2, J2, K3

OUT_FPD[13..0] : J3, K4, J4, H4, K5, J5, H5, K6, J6, H6, K7, J7, H7, G8

CC[8..0] : A8, B8, A9, B10, B9, C10, C9, D10, D9

CF[13..0] : E10, E9, F10, F9, G10, G9, H10, H9, J10, J9, K10, K9, J8, K8

Annex 11 : Pin out of the Input component (top view)

	A	B	C	D	E	F	G	H	J	K
1	TDI	CFPD0	CCED0	CCOINC	ETAT1	RAZ/ME	DCED0	DCED2	DCED4	DCED5
2	CFPD1	CCED1	CFPD2	CCED2	SCED	SCOINC	DCED1	DCED3	DCED7	DCED6
3	CFPD3	CCED3	Gnd	CFPD4	CCED4	TMS	SFPD	Vcc I/O	DFPD0	DCED8
4	CFPD5	CCED5	CFPD6	Vcc I/O	CCED6	ETAT2	Gnd	DFPD3	DFPD2	DFPD1
5	BPO1	RBPO1	CFPD7	Vcc core	Gnd	Vcc I/O	Gnd	DFPD6	DFPD5	DFPD4
6	STROBE	CCED7	CFPD8	Gnd	Vcc I/O	Gnd	Vcc core	DFPD9	DFPD8	DFPD7
7	CCED8	CFPD9	CFPD10	Gnd	CFPD11	DCOINC	Vcc I/O	DFPD12	DFPD11	DFPD10
8	CC0	CC1	Vcc I/O	CFPD12	CFPD13	TCK	DFPD13	Gnd	CF12	CF13
9	CC2	CC4	CC6	CC8	CF1	CF3	CF5	CF7	CF9	CF11
10	TDO	CC3	CC5	CC7	CF0	CF2	CF4	CF6	CF8	CF10

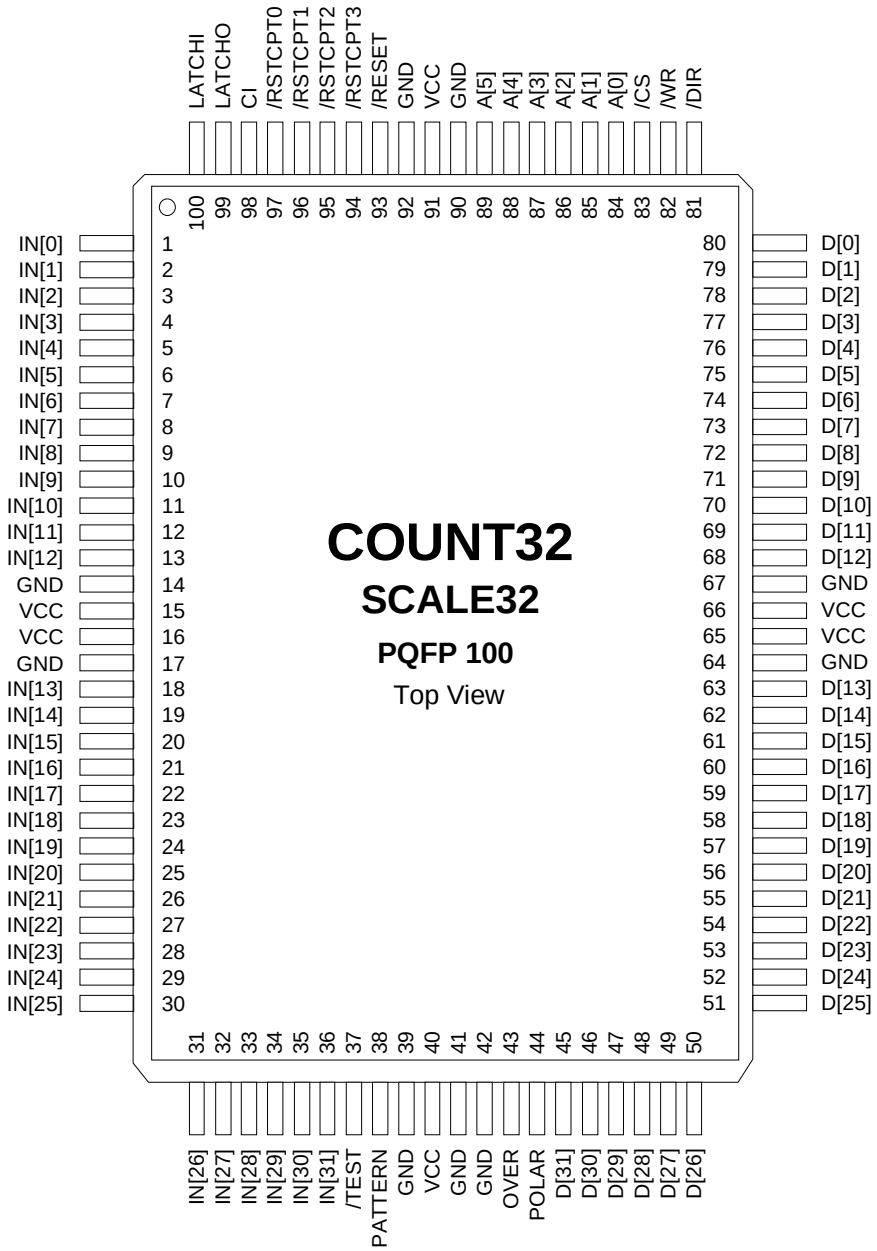
Top view

Annex 12 : Pin out of the INPUT component (bottom view)

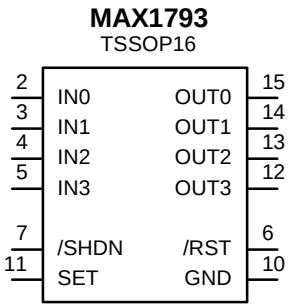
	K	J	H	G	F	E	D	C	B	A
1	DCED5	DCED4	DCED2	DCED0	RAZ/ME	ETAT1	CCOINC	CCED0	CFPD0	TDI
2	DCED6	DCED7	DCED3	DCED1	SCOINC	SCED	CCED2	CFPD2	CCED1	CFPD1
3	DCED8	DFPD0	Vcc I/O	SFPD	TMS	CCED4	CFPD4	Gnd	CCED3	CFPD3
4	DFPD1	DFPD2	DFPD3	Gnd	ETAT2	CCED6	Vcc I/O	CFPD6	CCED5	CFPD5
5	DFPD4	DFPD5	DFPD6	Gnd	Vcc I/O	Gnd	Vcc core	CFPD7	RBPO1	BPO1
6	DFPD7	DFPD8	DFPD9	Vcc core	Gnd	Vcc I/O	Gnd	CFPD8	CCED7	STROBE
7	DFPD10	DFPD11	DFPD12	Vcc I/O	DCOINC	CFPD11	Gnd	CFPD10	CFPD9	CCED8
8	CF13	CF12	Gnd	DFPD13	TCK	CFPD13	CFPD12	Vcc I/O	CC1	CC0
9	CF11	CF9	CF7	CF5	CF3	CF1	CC8	CC6	CC4	CC2
10	CF10	CF8	CF6	CF4	CF2	CF0	CC7	CC5	CC3	TDO

Bottom view

Annex 13 : Pin out of the COUNT32 component



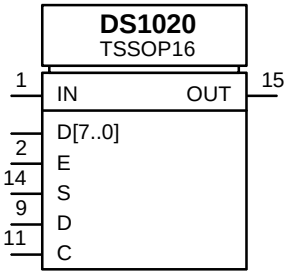
Annex 14 : 3,3V voltage regulator body component



N.C. : 1, 8, 9, 16

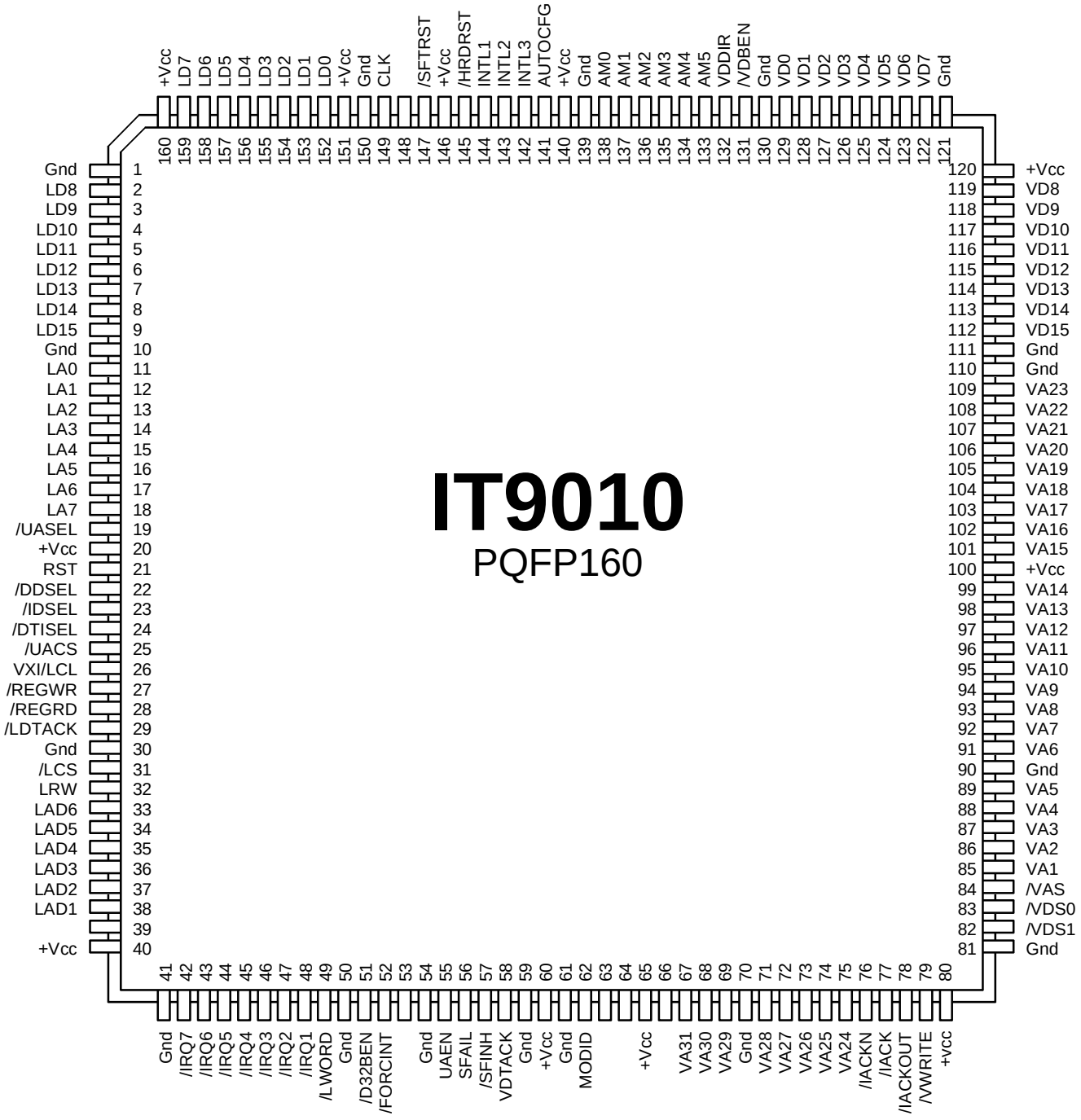
Warning : the package have an exposed thermal pad on its underside which must be connect to GND.

Annex 15 : Delay line body component

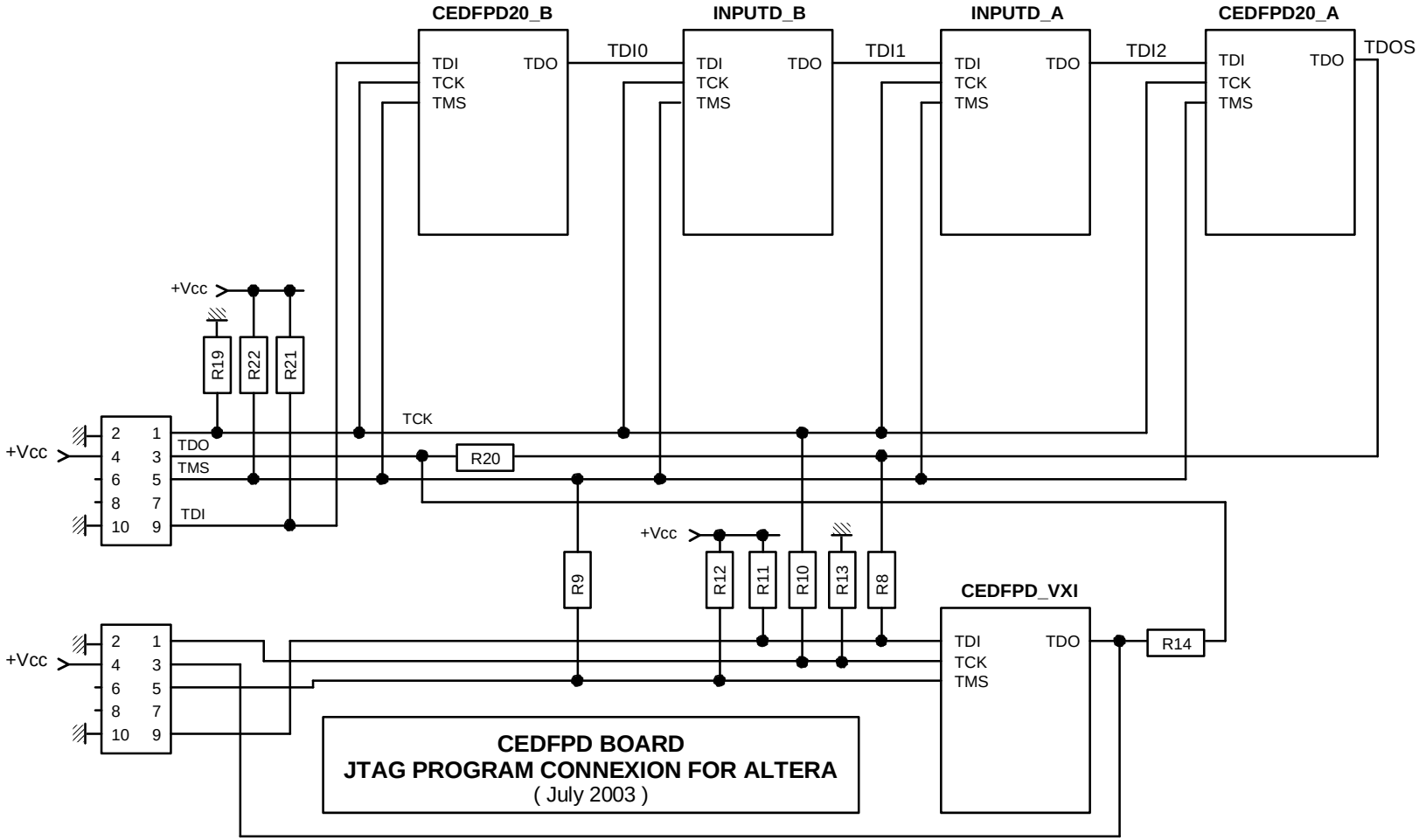


Gnd : 8
Vcc : 16
D[7..0] : 3, 4, 5, 6, 7, 10, 12, 13

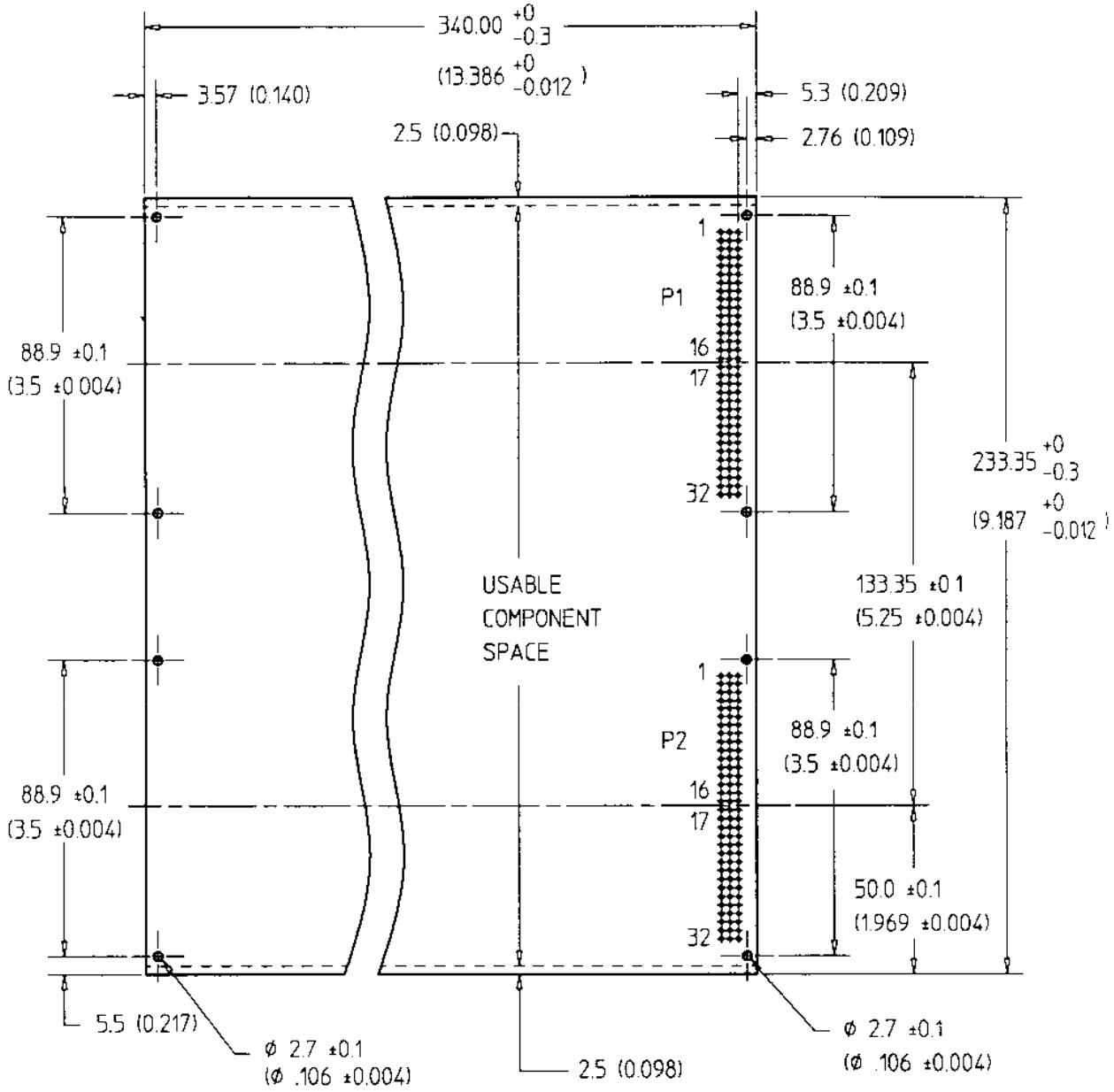
Annex 16 : IT9010 VXI Interface Chip pin out



Annex 17 : JTAG Program Connexion for FPGA ALTERA



Annex 18 : Mechanical Size C board

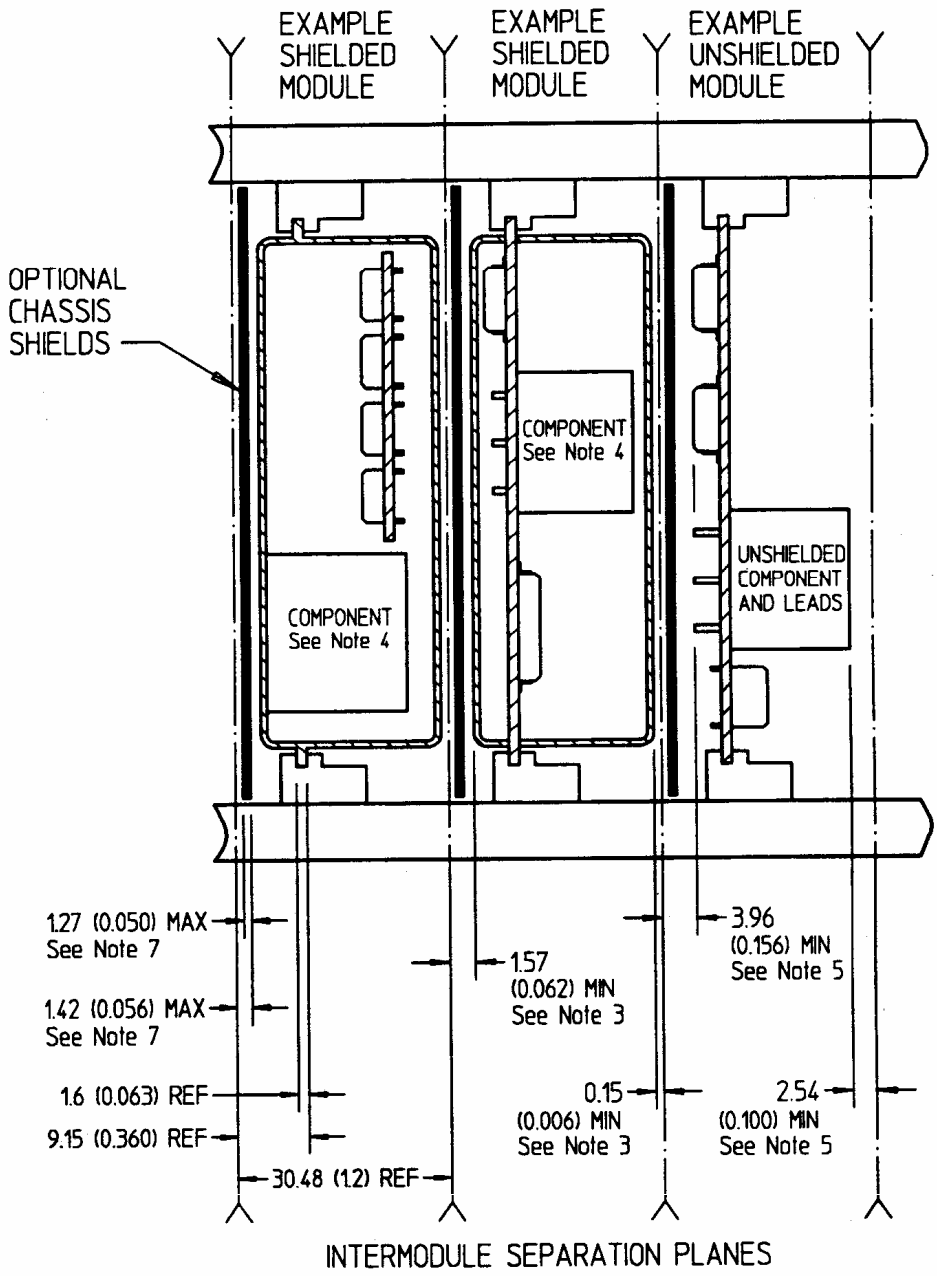


NOTES:

1. All dimensions are shown in millimeters.
   Inch dimensions are shown in parentheses
2. Front panel mounting holes are suggestions only.
3. OBSERVATION: P1 is required for VXI devices. P2 is optional.
4. OBSERVATION: Board outline may be reduced to accommodate shields.

Size C board

Annex 19 : VXI module envelope

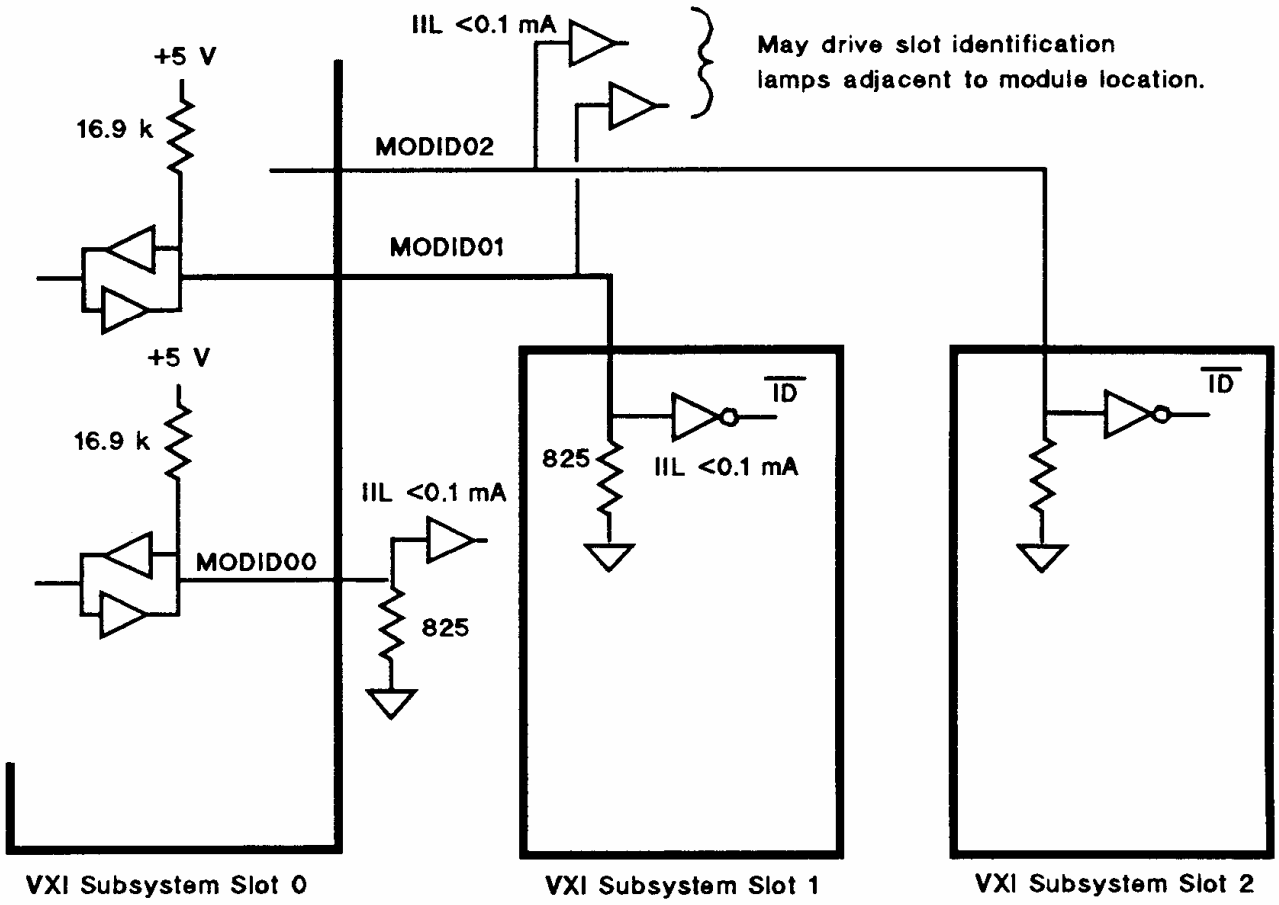


NOTES:

1. All dimensions are shown in millimeters. Inch dimensions are shown in parentheses.
2. Refer to the section, "Component Height, Lead Length, Shield Height and Warpage".
3. Minimum shield clearance refers to module when installed and includes the effects of warpage. RECOMMENDATION: Nominal clearance should be at least 0.5 (0.020) greater.
4. No restrictions are placed on components inside a shielded module.
5. Applies only to unshielded components and leads.
6. OBSERVATION: Extreme care must be taken with unshielded modules. Safety, handling, voltage, warpage, etc. should be considered.
7. RULE: IF provided, THEN the chassis shield MUST conform to these dimensions.

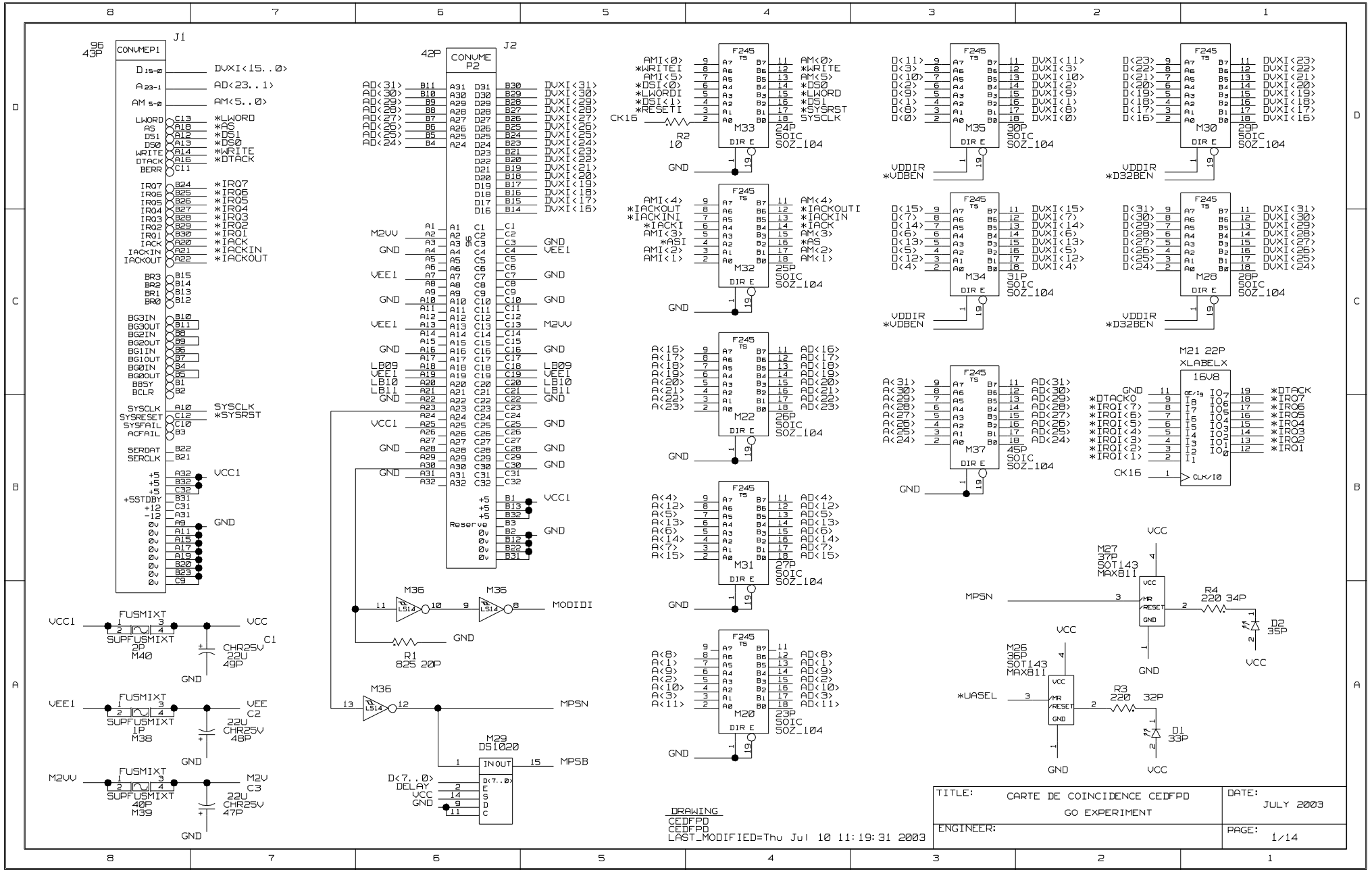
Module envelope, front view

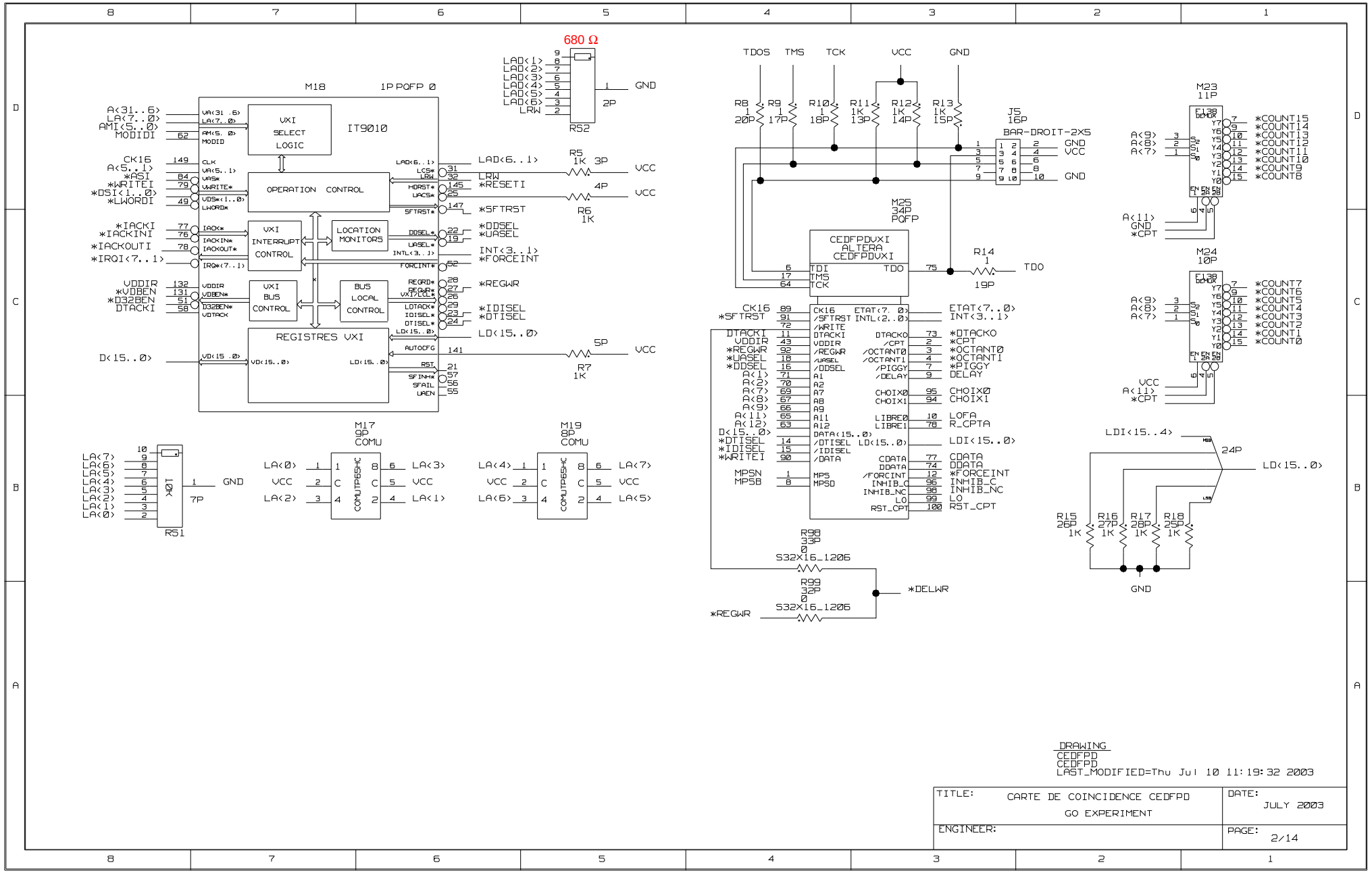
Annex 20 : ID line Module



Module ID lines.

Annex 21 : CEDFPD Board scheme




680 Ω
M18
1P PQFP 0
IT9010
VXI SELECT LOGIC
OPERATION CONTROL
VXI INTERRUPT CONTROL
LOCATION MONITORS
VXI BUS CONTROL
BUS LOCAL CONTROL
REGISTRES VXI
RS2
R5 1K 3P
R6 1K 4P
R7 1K 5P
M17 9P COMU
M19 8P COMU
RS1 10K 7P
M25 34P PQFP
CEDFPDVXI ALTERA CEDFPDVXI
R8 20P
R9 17P
R10 18P
R11 1K 13P
R12 1K 14P
R13 1K 15P
J5 16P BAR-DROIT-2X5
R14 1 19P
M23 11P
M24 10P
R15 26P 1K
R16 27P 1K
R17 28P 1K
R18 25P 1K
24P
R98 33P 0 S32X16_1206
R99 33P 0 S32X16_1206
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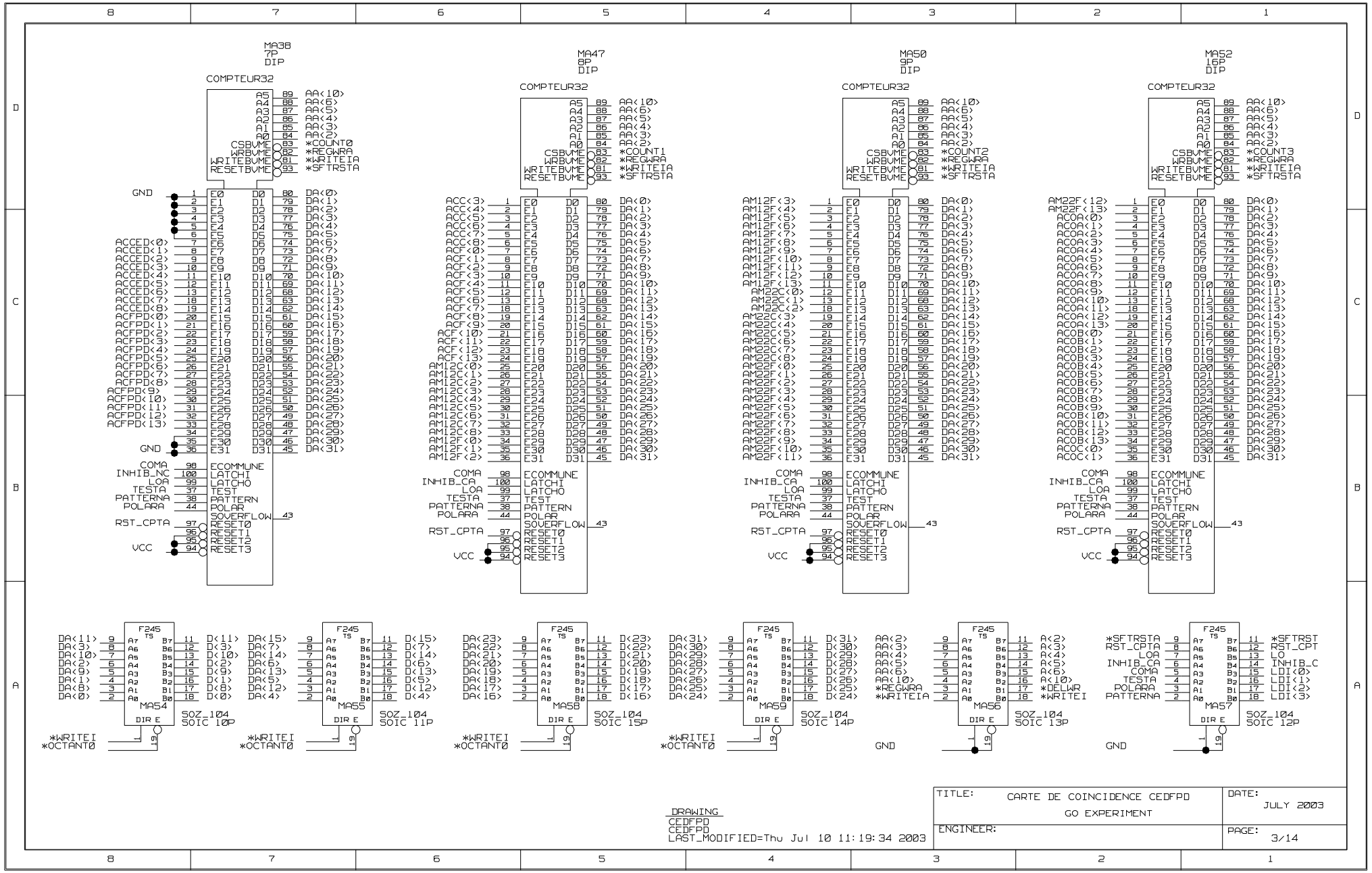
DATE: JULY 2003
ENGINEER:
PAGE: 2/14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7P
DIP
COMPTEUR32
MA47
8P
DIP
COMPTEUR32
MA50
9P
DIP
COMPTEUR32
MA52
16P
DIP
COMPTEUR32
ECOMMUNE
LATCHI
LATCHO
TEST
PATTERN
POLAR
SOVERFLOW
RESET0
RESET1
RESET2
RESET3
F245
MA54
SOZ_104
SOIC 10P
MA55
SOZ_104
SOIC 11P
MA58
SOZ_104
SOIC 15P
MA59
SOZ_104
SOIC 14P
MA56
SOZ_104
SOIC 13P
MA57
SOZ_104
SOIC 12P
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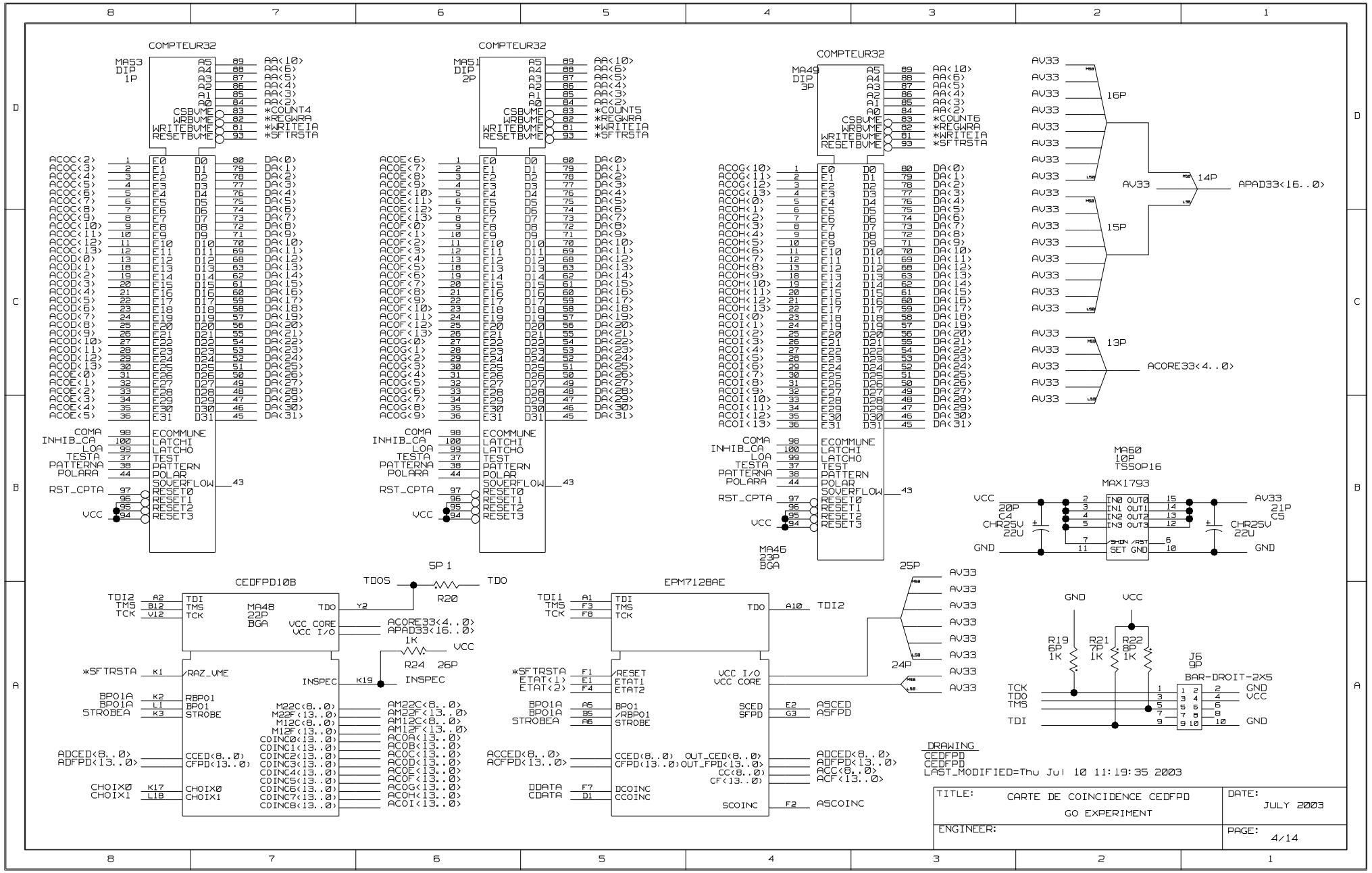
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MA53 DIP 1P
MA51 DIP 2P
MA49 DIP 3P
MA46 23P BGA
MA60 10P TSSOP16
MAX1793
CEDFPD10B
MA48 22P BGA
EPM7128AE
5P 1
R20
1K
R24 26P
16P
15P
14P
13P
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ACORE33<4..0>
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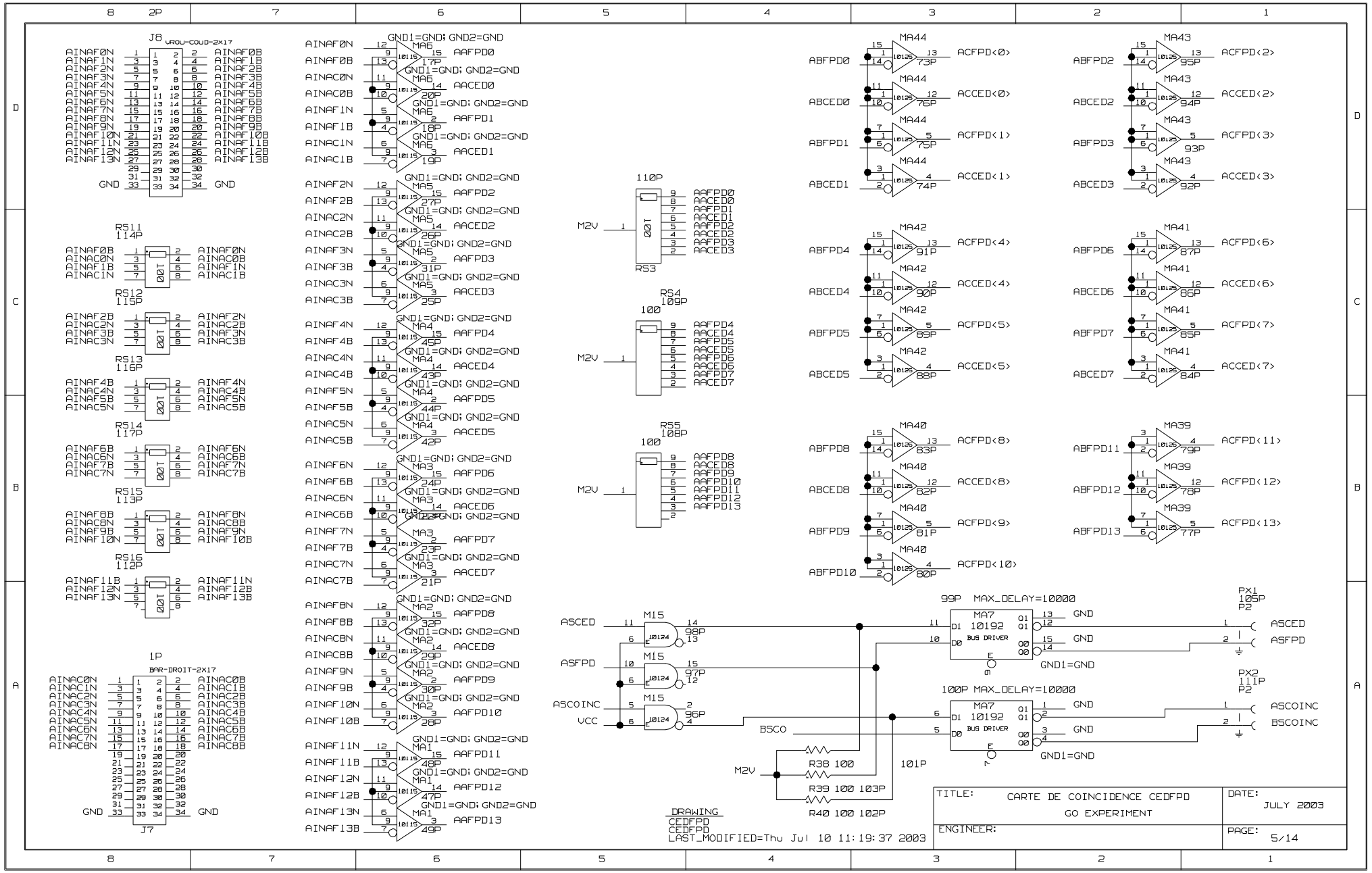
J8
VROU-COUD-2X17
RS11
114P
RS12
115P
RS13
116P
RS14
117P
RS15
113P
RS16
112P
1P
BAR-DROIT-2X17
J7
GND1=GND; GND2=GND
MA6
MA5
MA4
MA3
MA2
MA1
AAFPD0
AAFPD1
AAFPD2
AAFPD3
AAFPD4
AAFPD5
AAFPD6
AAFPD7
AAFPD8
AAFPD9
AAFPD10
AAFPD11
AAFPD12
AAFPD13
AACED0
AACED1
AACED2
AACED3
AACED4
AACED5
AACED6
AACED7
110P
RS3
RS4
109P
R55
108P
MA44
MA43
MA42
MA41
MA40
MA39
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ACCED<4>
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ACCED<8>
M15
MA7
10192
BUS DRIVER
99P MAX_DELAY=10000
100P MAX_DELAY=10000
PX1
105P
P2
PX2
111P
ASCED
ASFPD
ASCOINC
VCC
BSCO
R38 100
R39 100 103P
R40 100 102P
101P
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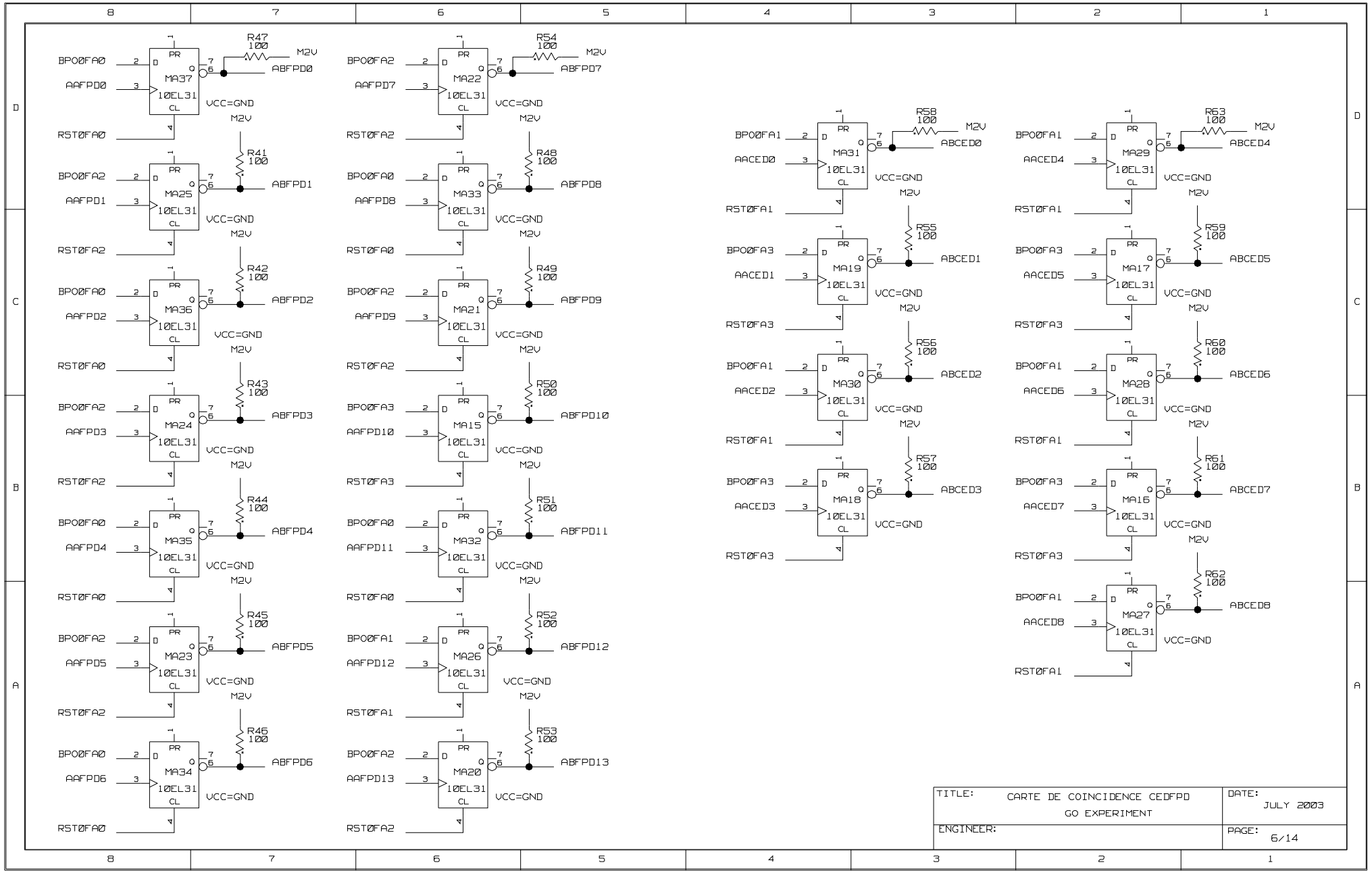
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R41 100 ABFPD1 BP00FA2 AAFPD1 RST0FA2 MA25 10EL31
R42 100 ABFPD2 BP00FA0 AAFPD2 RST0FA0 MA36 10EL31
R43 100 ABFPD3 BP00FA2 AAFPD3 RST0FA2 MA24 10EL31
R44 100 ABFPD4 BP00FA0 AAFPD4 RST0FA0 MA35 10EL31
R45 100 ABFPD5 BP00FA2 AAFPD5 RST0FA2 MA23 10EL31
R46 100 ABFPD6 BP00FA0 AAFPD6 RST0FA0 MA34 10EL31
R54 100 M2V ABFPD7 BP00FA2 AAFPD7 RST0FA2 MA22 10EL31
R48 100 ABFPD8 BP00FA0 AAFPD8 RST0FA0 MA33 10EL31
R49 100 ABFPD9 BP00FA2 AAFPD9 RST0FA2 MA21 10EL31
R50 100 ABFPD10 BP00FA3 AAFPD10 RST0FA3 MA15 10EL31
R51 100 ABFPD11 BP00FA0 AAFPD11 RST0FA0 MA32 10EL31
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R53 100 ABFPD13 BP00FA2 AAFPD13 RST0FA2 MA20 10EL31
R58 100 M2V ABCED0 BP00FA1 AACED0 RST0FA1 MA31 10EL31
R55 100 ABCED1 BP00FA3 AACED1 RST0FA3 MA19 10EL31
R56 100 ABCED2 BP00FA1 AACED2 RST0FA1 MA30 10EL31
R57 100 ABCED3 BP00FA3 AACED3 RST0FA3 MA18 10EL31
R63 100 M2V ABCED4 BP00FA1 AACED4 RST0FA1 MA29 10EL31
R59 100 ABCED5 BP00FA3 AACED5 RST0FA3 MA17 10EL31
R60 100 ABCED6 BP00FA1 AACED6 RST0FA1 MA28 10EL31
R61 100 ABCED7 BP00FA3 AACED7 RST0FA3 MA16 10EL31
R62 100 ABCED8 BP00FA1 AACED8 RST0FA1 MA27 10EL31
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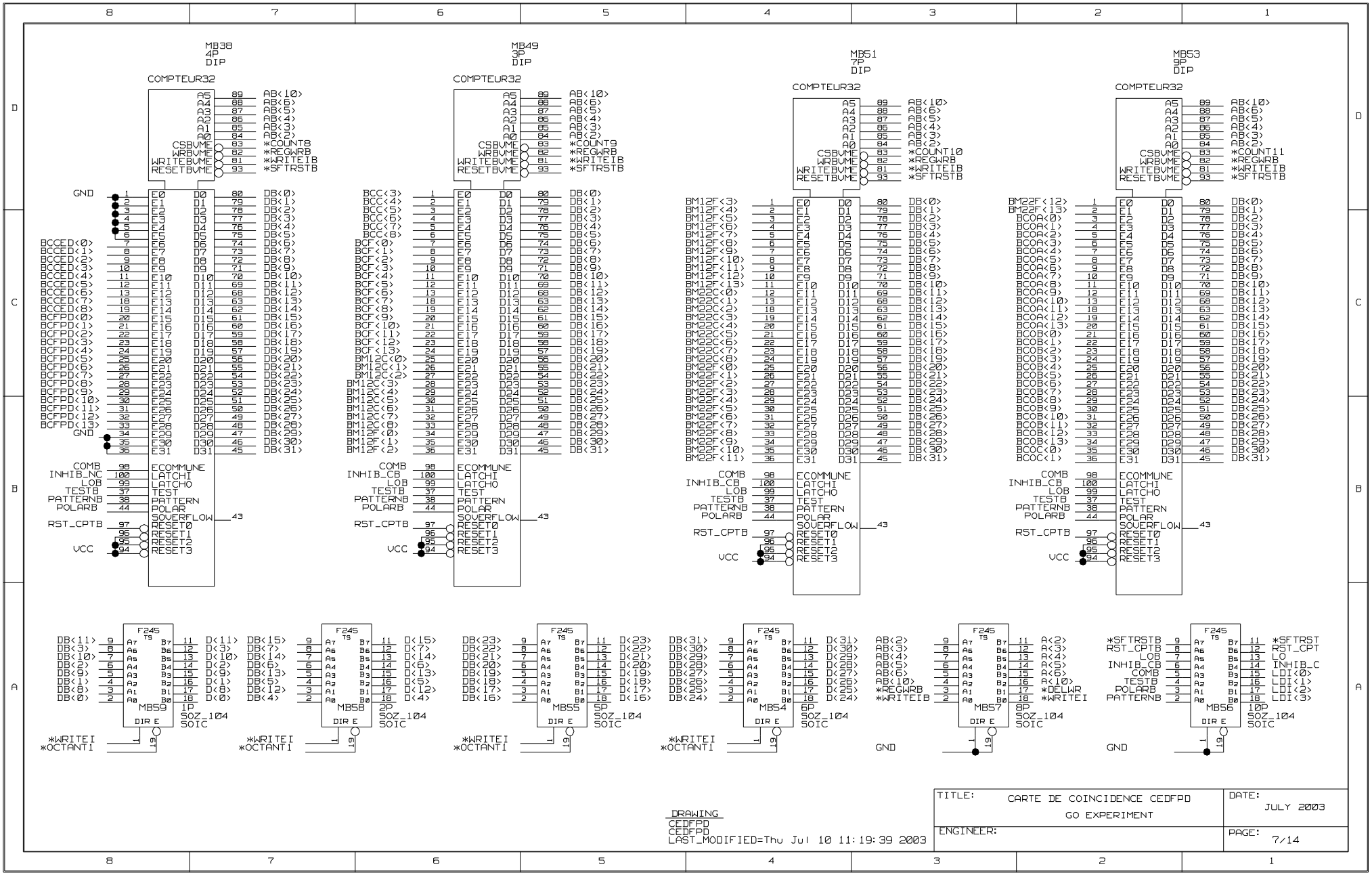
PAGE: 6/14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DIP
COMPTEUR32
MB49
3P
DIP
COMPTEUR32
MB51
7P
DIP
COMPTEUR32
MB53
9P
DIP
COMPTEUR32
ECOMMUNE
LATCHI
LATCHO
TEST
PATTERN
POLAR
SOVERFLOW
RESET0
RESET1
RESET2
RESET3
F245
MB59
1P
SOZ_104
SOIC
MB58
2P
SOZ_104
SOIC
MB55
5P
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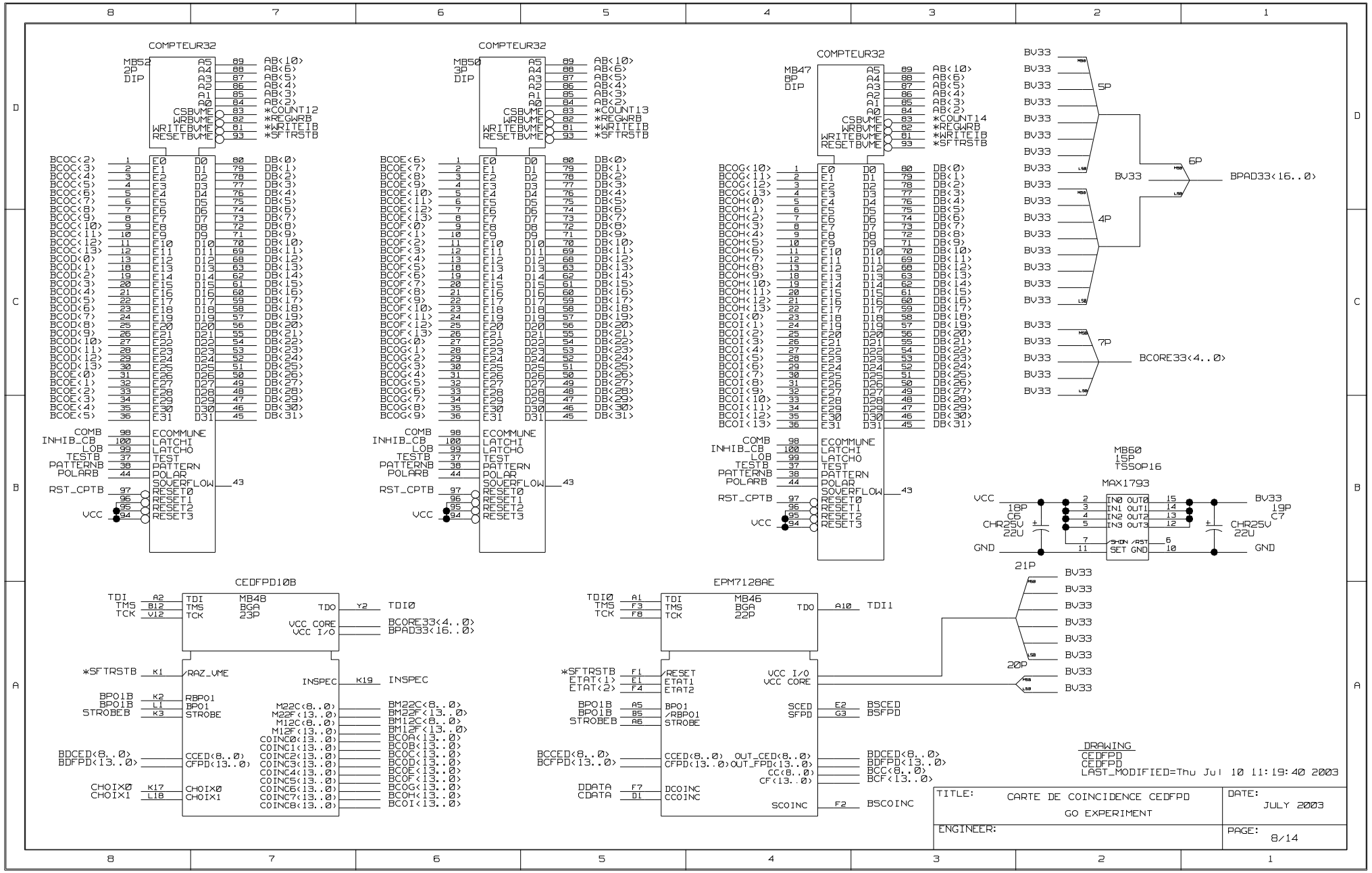
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MB50 3P DIP
MB47 6P DIP
CEDFPD10B
MB48 BGA 23P
EPM7128AE
MB46 BGA 22P
MB60 15P TSSOP16
MAX1793
5P
6P
4P
7P
18P C6 CHR25V 22U
19P C7 CHR25V 22U
21P
20P
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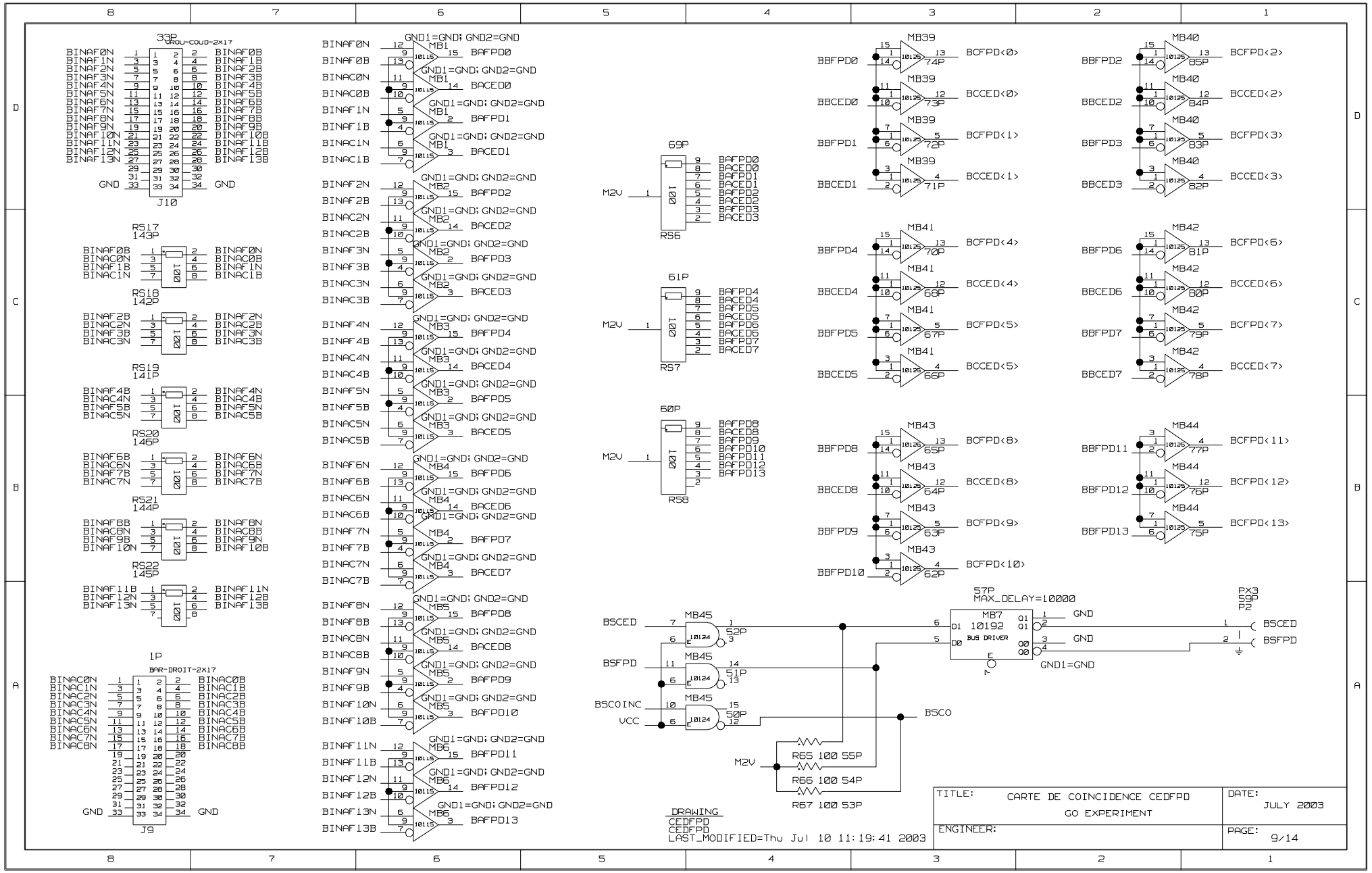
33P
CAROU-COUD-2X17
J10
R517
143P
R518
142P
R519
141P
R520
146P
R521
144P
R522
145P
1P
BAR-DROIT-2X17
J9
MB1
MB2
MB3
MB4
MB5
MB6
69P
RS6
61P
RS7
60P
RS8
MB39
MB40
MB41
MB42
MB43
MB44
MB45
MB7
10192
BUS DRIVER
57P
MAX_DELAY=10000
PX3
59P
P2
R65 100 55P
R66 100 54P
R67 100 53P
M2V
VCC
GND
GND1=GND
BSCED
BSFPD
BSCOINC
BSCO
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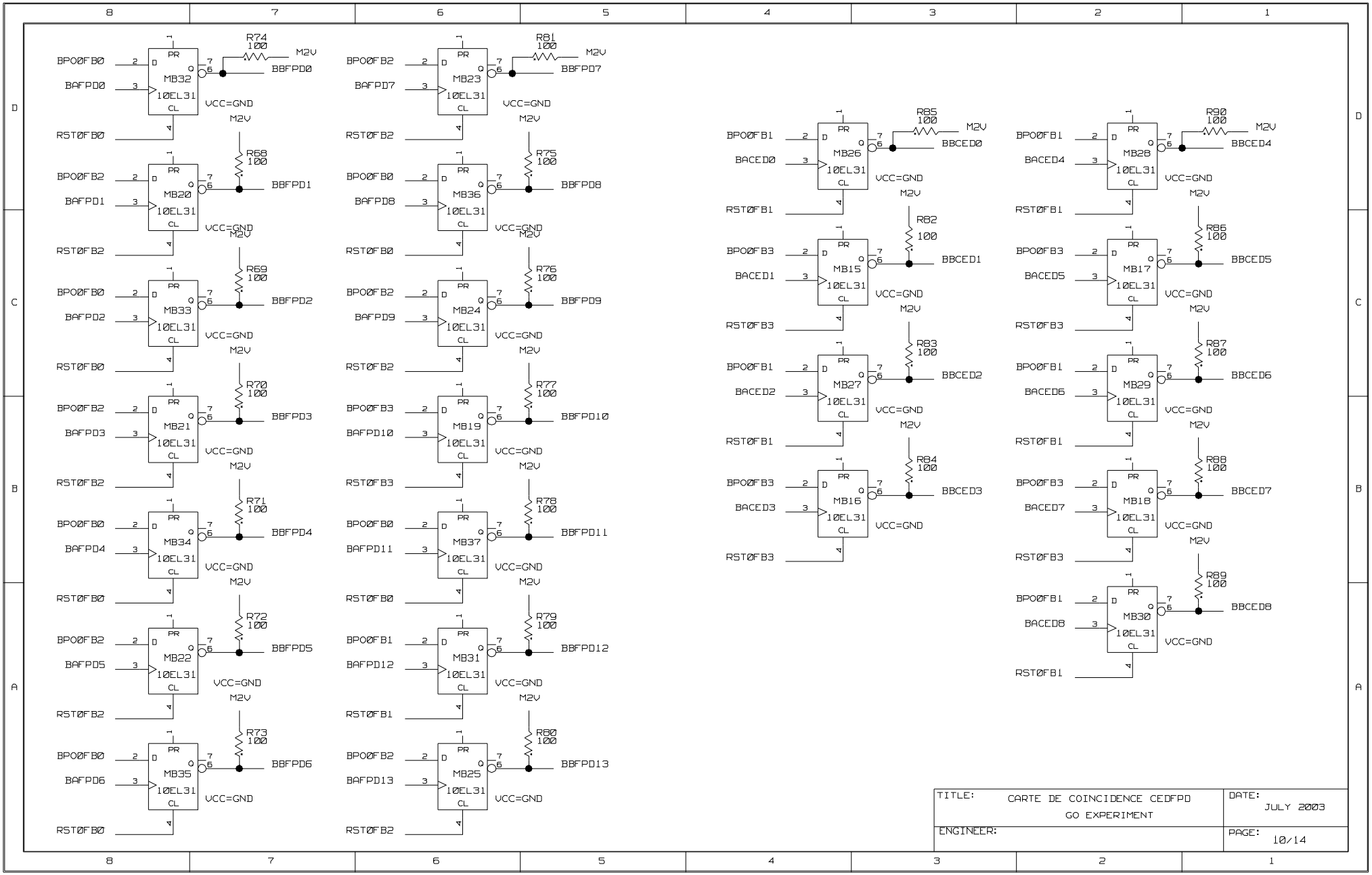
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R68 100 BBFPD1 BPØØFB2 BAFPD1 MB20 10EL31 VCC=GND RSTØFB2
R69 100 BBFPD2 BPØØFBØ BAFPD2 MB33 10EL31 VCC=GND RSTØFBØ
R70 100 BBFPD3 BPØØFB2 BAFPD3 MB21 10EL31 VCC=GND RSTØFB2
R71 100 BBFPD4 BPØØFBØ BAFPD4 MB34 10EL31 VCC=GND RSTØFBØ
R72 100 BBFPD5 BPØØFB2 BAFPD5 MB22 10EL31 VCC=GND RSTØFB2
R73 100 BBFPD6 BPØØFBØ BAFPD6 MB35 10EL31 VCC=GND RSTØFBØ
R81 100 M2V BBFPD7 BPØØFB2 BAFPD7 MB23 10EL31 VCC=GND RSTØFB2
R75 100 BBFPD8 BPØØFBØ BAFPD8 MB36 10EL31 VCC=GND RSTØFBØ
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R77 100 BBFPD10 BPØØFB3 BAFPD10 MB19 10EL31 VCC=GND RSTØFB3
R78 100 BBFPD11 BPØØFBØ BAFPD11 MB37 10EL31 VCC=GND RSTØFBØ
R79 100 BBFPD12 BPØØFB1 BAFPD12 MB31 10EL31 VCC=GND RSTØFB1
R80 100 BBFPD13 BPØØFB2 BAFPD13 MB25 10EL31 VCC=GND RSTØFB2
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R83 100 BBCED2 BPØØFB1 BACED2 MB27 10EL31 VCC=GND RSTØFB1
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R87 100 BBCED6 BPØØFB1 BACED6 MB29 10EL31 VCC=GND RSTØFB1
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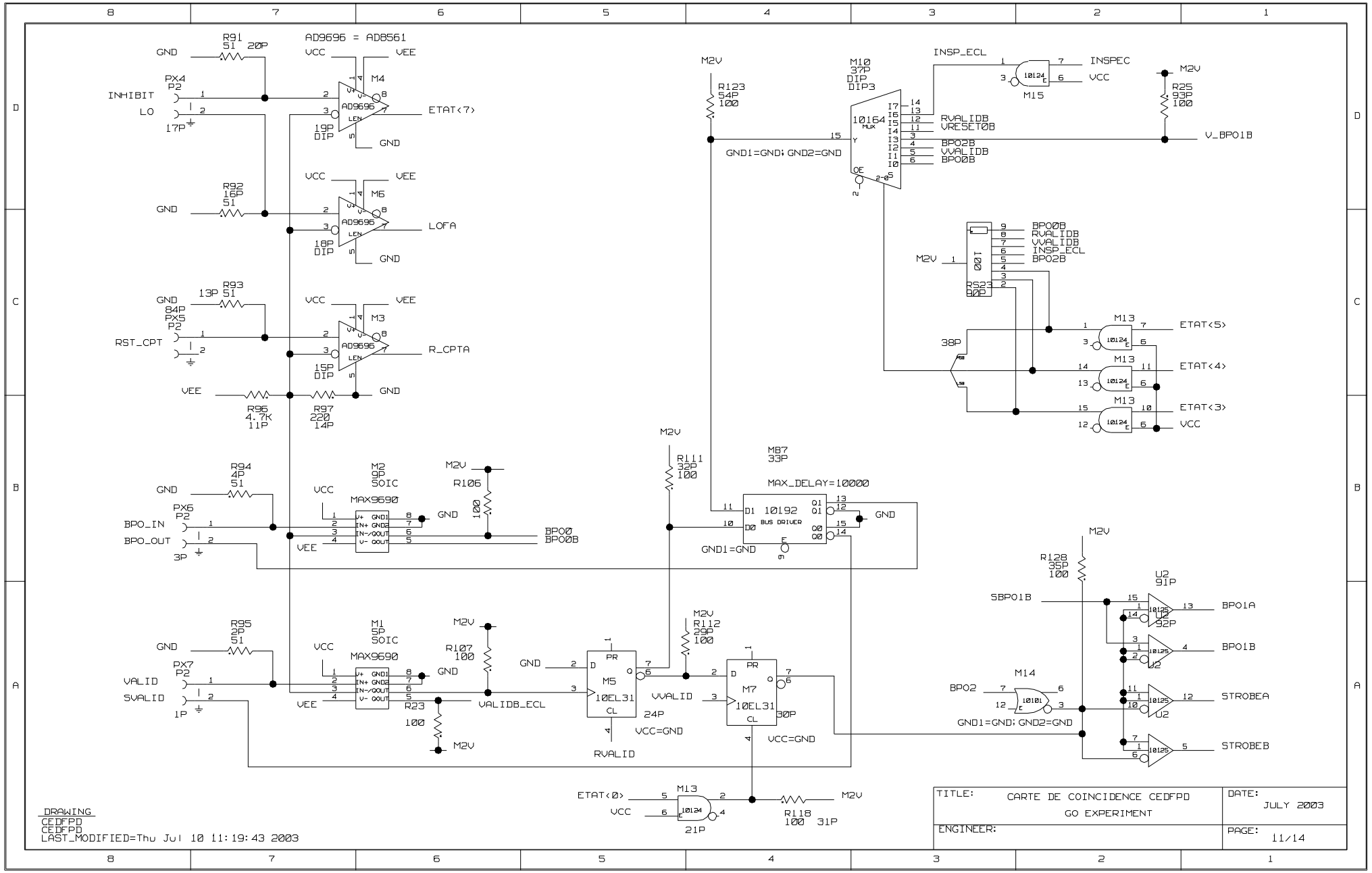
PAGE: 10/14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LO
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VCC
VEE
M4
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19P DIP
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M6
LOFA
18P DIP
R93 13P 51
PX5 P2
RST_CPT
M3
R_CPTA
15P DIP
R96 4.7K 11P
R97 220 14P
R94 4P 51
PX6 P2
BPO_IN
BPO_OUT
3P
M2 9P SOIC
MAX9690
R106 100
BPØ
BPØB
R95 2P 51
PX7 P2
VALID
SVALID
1P
M1 5P SOIC
R107 100
R23 100
VALIDB_ECL
M2V
R123 54P 100
GND1=GND; GND2=GND
M10 37P DIP DIP3
10164 MUX
RVALIDB
VRESETØB
BPO2B
VVALIDB
BPOØB
INSP_ECL
M15
INSPEC
R25 93P 100
V_BPO1B
BPOØB
RVALIDB
VVALIDB
INSP_ECL
BPO2B
38P
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MB7 33P
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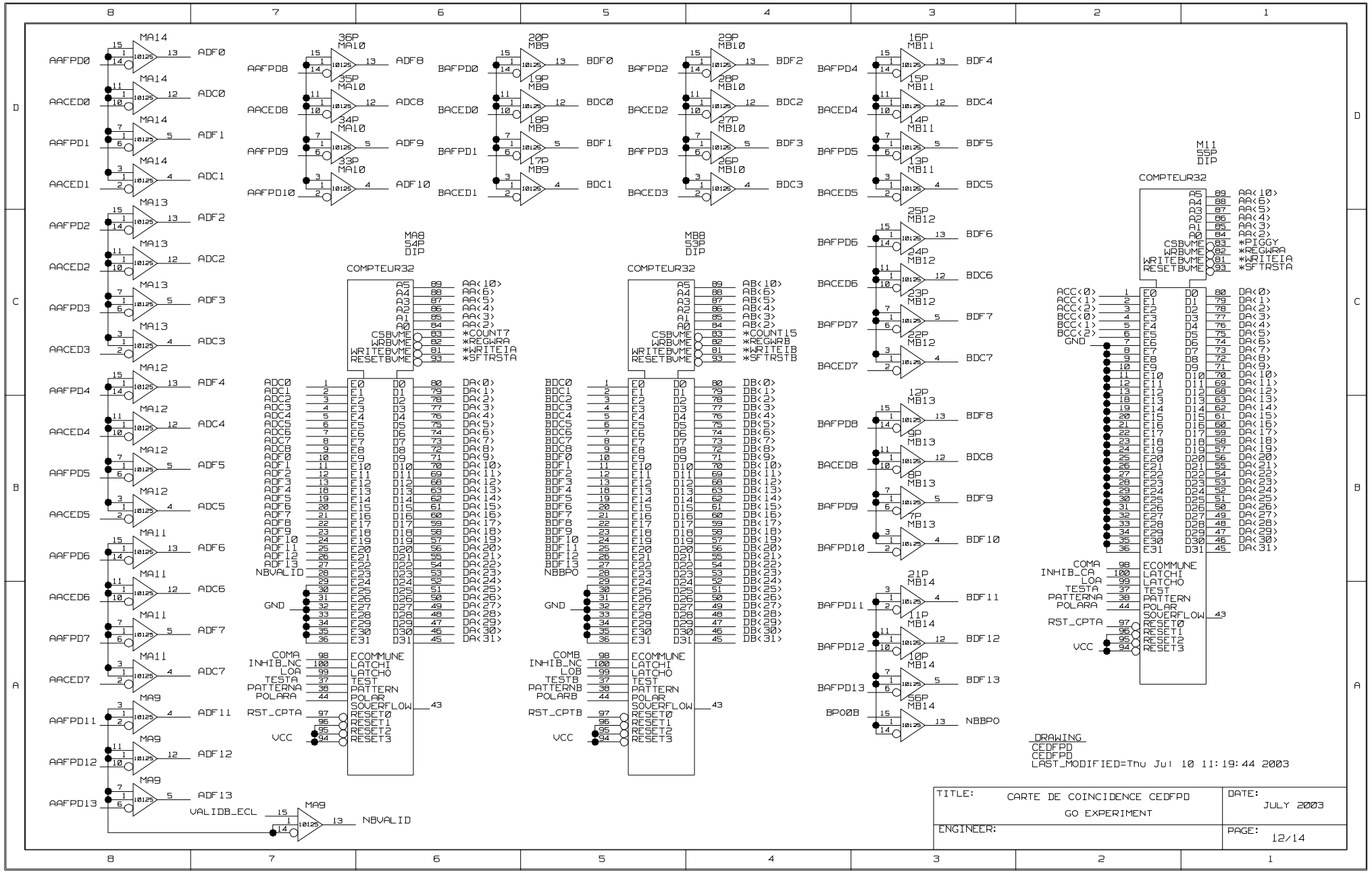
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MA13
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ADC2
AAFPD3
ADF3
AACED3
ADC3
MA12
AAFPD4
ADF4
AACED4
ADC4
AAFPD5
ADF5
AACED5
ADC5
MA11
AAFPD6
ADF6
AACED6
ADC6
AAFPD7
ADF7
AACED7
ADC7
MA9
AAFPD11
ADF11
AAFPD12
ADF12
AAFPD13
ADF13
VALIDB_ECL
NBVALID
36P
MA10
AAFPD8
ADF8
35P
MA10
AACED8
ADC8
34P
MA10
AAFPD9
ADF9
33P
MA10
AAFPD10
ADF10
20P
MB9
BAFPD0
BDF0
19P
MB9
BACED0
BDC0
18P
MB9
BAFPD1
BDF1
17P
MB9
BACED1
BDC1
29P
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BDF2
28P
MB10
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BDC2
27P
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26P
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BACED3
BDC3
16P
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BDF4
15P
MB11
BACED4
BDC4
14P
MB11
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BDC6
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AA<5>
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*REGWRA
*WRITEIA
*SFTRSTA
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ADC2
ADC3
ADC4
ADC5
ADC6
ADC7
ADC8
ADF0
ADF1
ADF2
ADF3
ADF4
ADF5
ADF6
ADF7
ADF8
ADF9
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ADF11
ADF12
ADF13
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TESTA
PATTERNA
POLARA
RST_CPTA
VCC
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LATCHI
LATCHO
TEST
PATTERN
POLAR
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RESETI
RESET2
RESET3
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BDC4
BDC5
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BDC7
BDC8
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BDF1
BDF2
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TESTB
PATTERNB
POLARB
RST_CPTB
VCC
ECOMMUNE
LATCHI
LATCHO
TEST
PATTERN
POLAR
SOVERFLOW
RESET0
RESETI
RESET2
RESET3
M11
55P
DIP
COMPTEUR32
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AA<6>
AA<5>
AA<4>
AA<3>
AA<2>
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*REGWRA
*WRITEIA
*SFTRSTA
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WRBVME
WRITEBVME
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LOA
TESTA
PATTERNA
POLARA
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ECOMMUNE
LATCHI
LATCHO
TEST
PATTERN
POLAR
SOVERFLOW
RESET0
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RESET3
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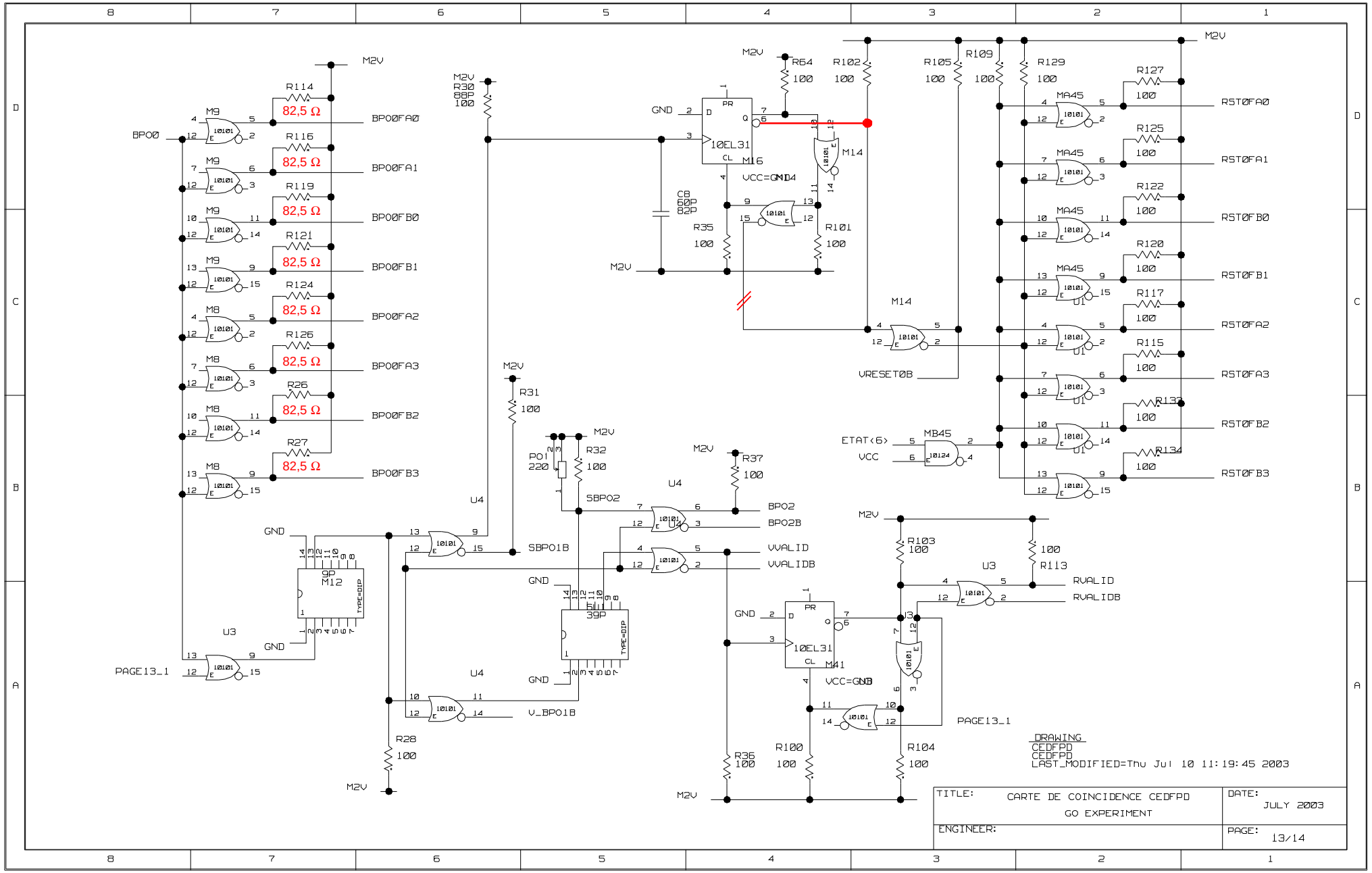
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R116
BP00FA1
R119
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R126
BP00FA3
R26
BP00FB2
R27
BP00FB3
BP00
M9
M8
R30
R64
100
R102
R105
R109
R129
R127
R125
R122
R120
R117
R115
R133
R134
MA45
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RST0FA1
RST0FB0
RST0FB1
RST0FA2
RST0FA3
RST0FB2
RST0FB3
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M16
M14
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82P
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R101
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VCC
MB45
R31
R32
PO1
220
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SBP01B
U4
R37
BP02
BP02B
VVALID
VVALIDB
M12
M11
39P
U3
R103
R113
RVALID
RVALIDB
M41
R36
R100
R104
R28
V_BP01B
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C9 10N VEE GND
C10 10N VEE GND
C11 10N VEE GND
C12 10N VEE GND
C13 10N VEE GND
C14 10N VEE GND
C15 10N VEE GND
C16 10N VEE GND
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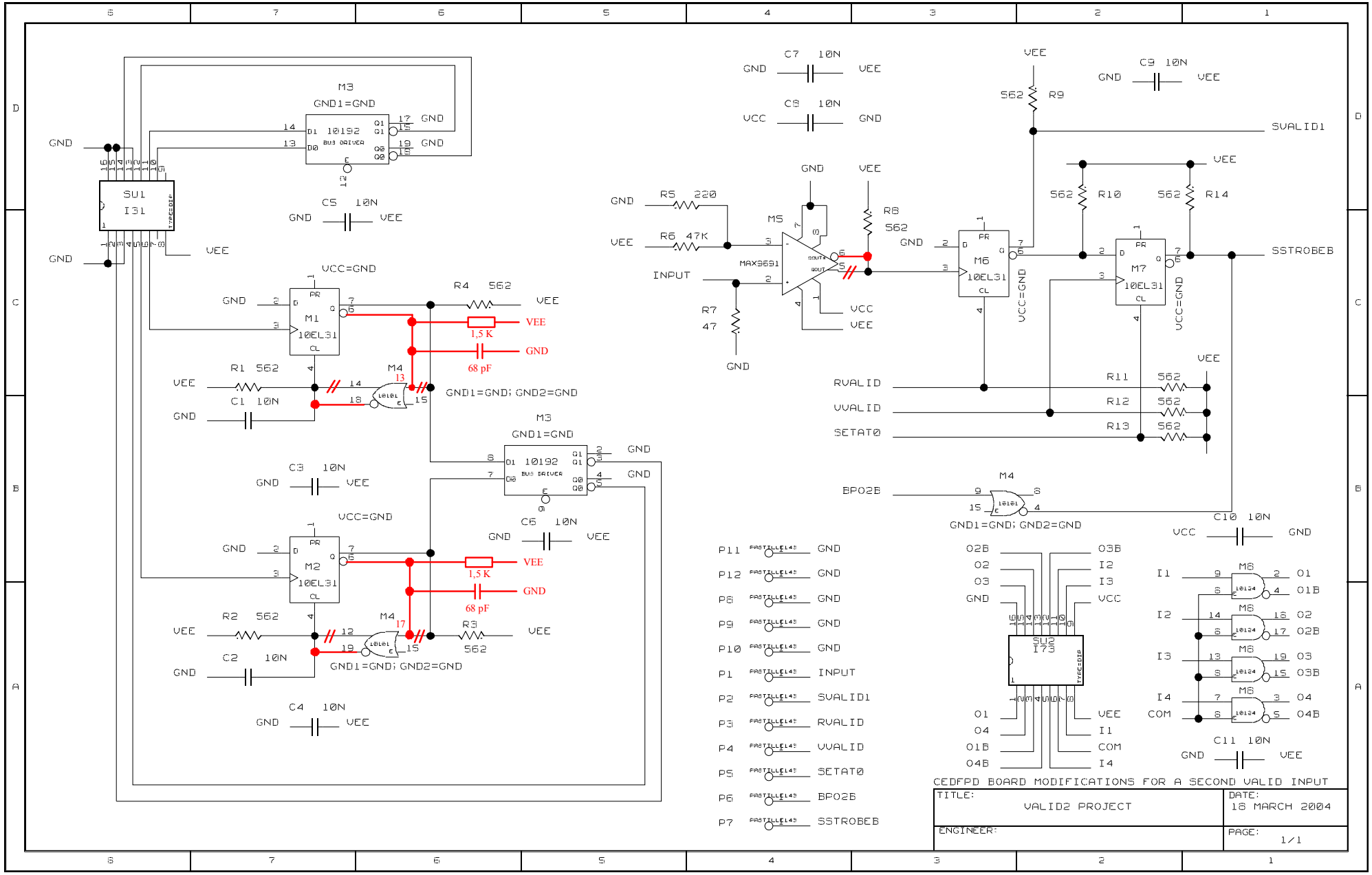
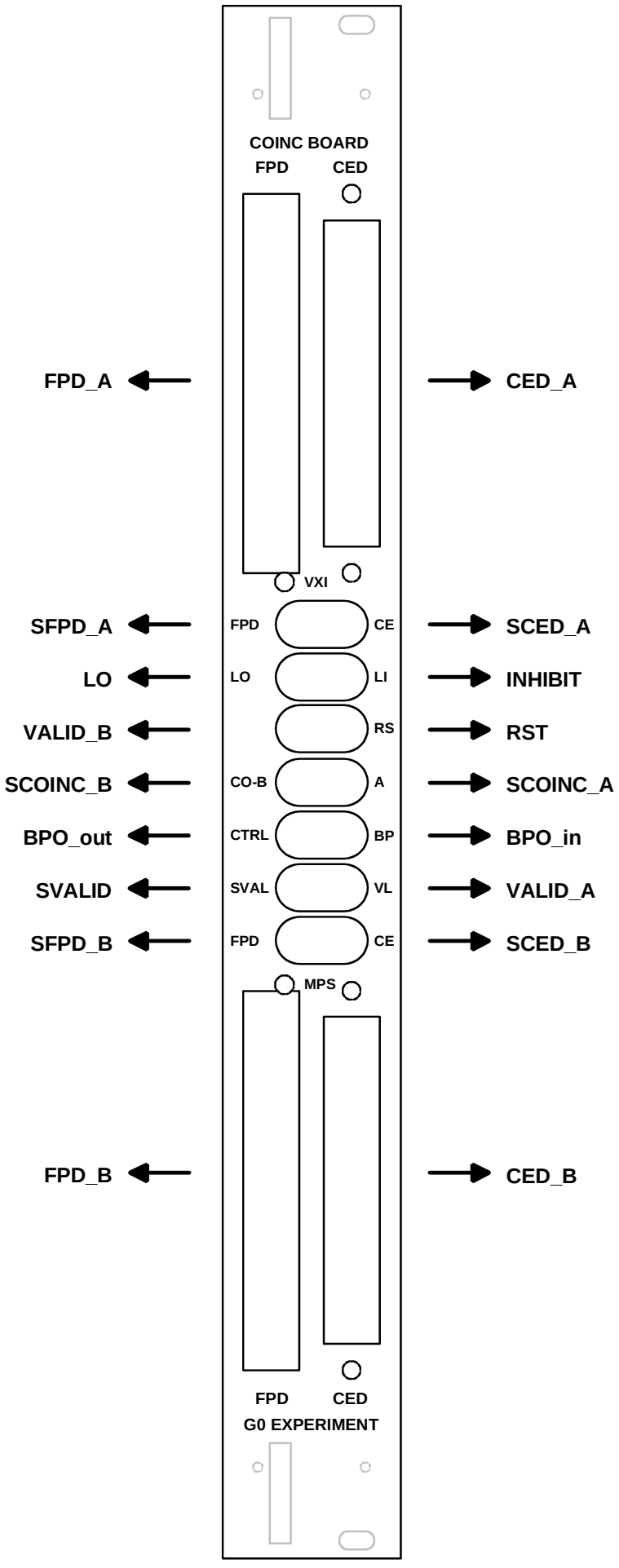
Annex 22 : CEDFPD_carte_fille board scheme



Annex 23 : Front Panel



Annex 24 : Interrupt vector address jump

Board Logical address	IT Address jump
0x”00”	0x”0000”
0x”01”	0x”0004”
0x”02”	0x”0008”
0x”03”	0x”000C”
0x”04”	0x”0010”
0x”05”	0x”0014”
0x”06”	0x”0018”
0x”07”	0x”001C”
0x”08”	0x”0020”
0x”09”	0x”0024”
0x”0A”	0x”0028”
0x”0B”	0x”002C”
0x”0C”	0x”0030”
0x”0D”	0x”0034”
0x”0E”	0x”0038”
0x”0F”	0x”003C”
0x”10”	0x”0040”
0x”11”	0x”0044”
0x”12”	0x”0048”
0x”13”	0x”004C”
0x”14”	0x”0050”
0x”15”	0x”0054”
0x”16”	0x”0058”
0x”17”	0x”005C”
0x”18”	0x”0060”
0x”19”	0x”0064”
0x”1A”	0x”0068”
0x”1B”	0x”006C”
0x”1C”	0x”0070”
0x”1D”	0x”0074”
0x”1E”	0x”0078”
0x”1F”	0x”007C”
0x”20”	0x”0080”
0x”21”	0x”0084”
0x”22”	0x”0088”
0x”23”	0x”008C”
0x”24”	0x”0090”
0x”25”	0x”0094”
0x”26”	0x”0098”
0x”27”	0x”009C”
0x”28”	0x”00A0”
0x”29”	0x”00A4”
0x”2A”	0x”00A8”
0x”2B”	0x”00AC”
0x”2C”	0x”00B0”
0x”2D”	0x”00B4”
0x”2E”	0x”00B8”
0x”2F”	0x”00BC”
0x”30”	0x”00C0”
0x”31”	0x”00C4”
0x”32”	0x”00C8”
0x”33”	0x”00CC”
0x”34”	0x”00D0”
0x”35”	0x”00D4”
0x”36”	0x”00D8”
0x”37”	0x”00DC”
0x”38”	0x00E0”
0x”39”	0x”00E4”
0x”3A”	0x”00E8”
0x”3B”	0x”00EC”
0x”3C”	0x”00F0”
0x”3D”	0x”00F4”
0x”3E”	0x”00F8”
0x”3F”	0x”00FC”
0x»40”	0x”0100”
0x»41”	0x”0104”
0x»42”	0x”0108”
0x»43”	0x”010C”
0x»44”	0x”0110”
0x»45”	0x”0114”
0x»46”	0x”0118”
0x»47”	0x”011C”
0x»48”	0x”0120”
0x»49”	0x”0124”
0x»4A”	0x”0128”
0x»4B”	0x”012C”
0x»4C”	0x”0130”
0x»4D”	0x”0134”
0x»4E”	0x”0138”
0x»4F”	0x”013C”
0x»50”	0x”0140”
0x»51”	0x”0144”
0x»52”	0x”0148”
0x»53”	0x”014C”
0x»54”	0x”0150”
0x»55”	0x”0154”
0x»56”	0x”0158”
0x»57”	0x”015C”
0x»58”	0x”0160”
0x»59”	0x”0164”
0x»5A”	0x”0168”
0x»5B”	0x”016C”
0x»5C”	0x”0170”
0x»5D”	0x”0174”
0x»5E”	0x”0178”
0x»5F”	0x”017C”
0x»60”	0x”0180”
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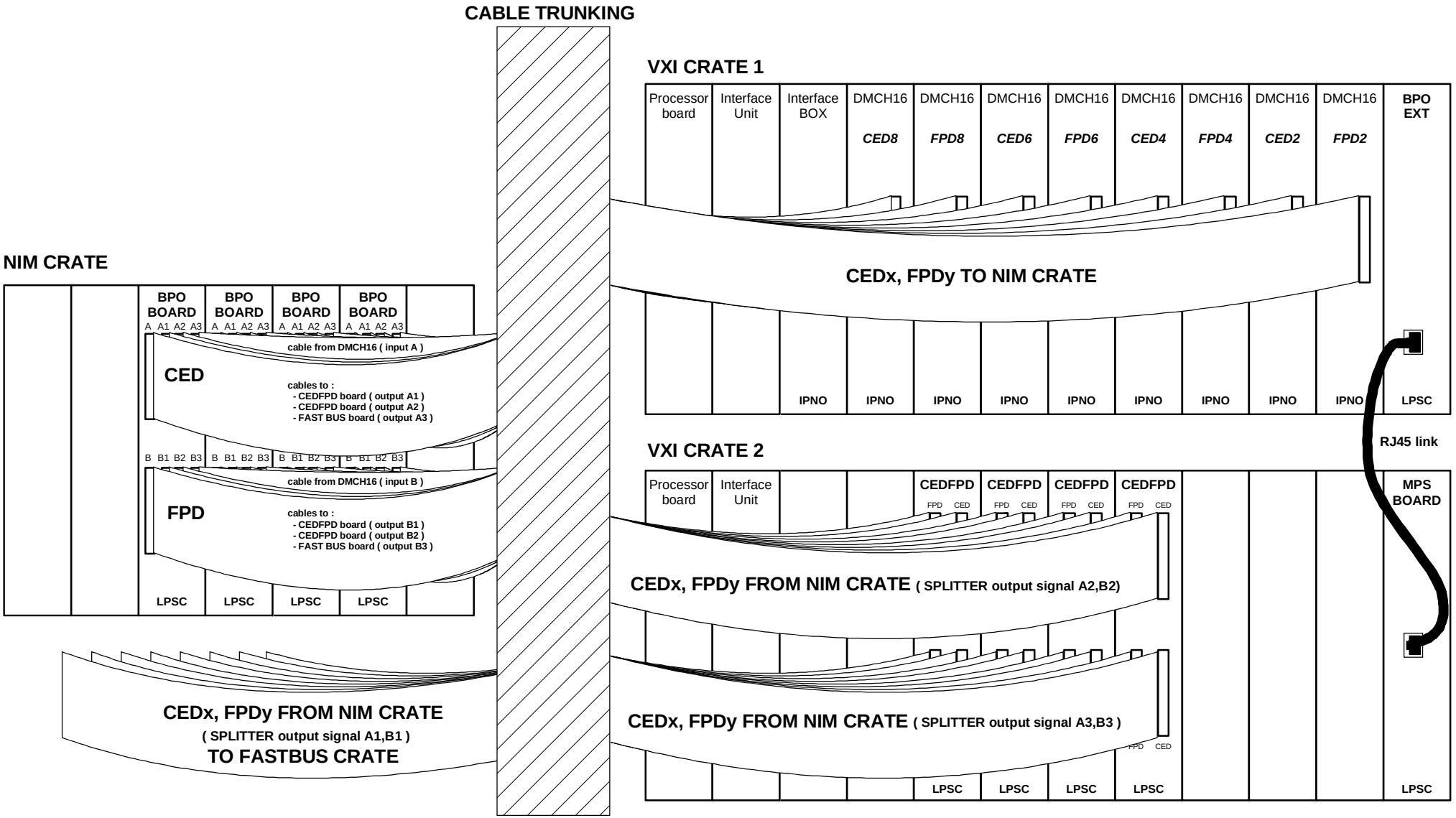
0x»62”	0x”0188”
0x»63”	0x”018C”
0x»64”	0x”0190”
0x»65”	0x”0194”
0x»66”	0x”0198”
0x»67”	0x”019C”
0x»68”	0x”01A0”
0x»69”	0x”01A4”
0x»6A”	0x”01A8”
0x»6B”	0x”01AC”
0x»6C”	0x”01B0”
0x»6D”	0x”01B4”
0x»6E”	0x”01B8”
0x»6F”	0x”01BC”
0x»70”	0x”01C0”
0x»71”	0x”01C4”
0x»72”	0x”01C8”
0x»73”	0x”01CC”
0x»74”	0x”01D0”
0x»75”	0x”01D4”
0x»76”	0x”01D8”
0x»77”	0x”01DC”
0x»78”	0x”01E0”
0x»79”	0x”01E4”
0x»7A”	0x”01E8”
0x»7B”	0x”01EC”
0x»7C”	0x”01F0”
0x»7D”	0x”01F4”
0x»7E”	0x”01F8”
0x»7F”	0x”01FC”
0x»80”	0x”0200”
0x»81”	0x”0204”
0x»82”	0x”0208”
0x»83”	0x”020C”
0x»84”	0x”0210”
0x»85”	0x”0214”
0x»86”	0x”0218”

Board Logical address	IT Address jump
0x»87”	0x”021C”
0x»88”	0x”0220”
0x»89”	0x”0224”
0x»8A”	0x”0228”
0x»8B”	0x”022C”
0x»8C”	0x”0230”
0x»8D”	0x”0234”
0x»8E”	0x”0238”
0x»8F”	0x”023C”
0x»90”	0x”0240”
0x»91”	0x”0244”
0x»92”	0x”0248”
0x»93”	0x”024C”
0x»94”	0x”0250”
0x»95”	0x”0254”
0x»96”	0x”0258”
0x»97”	0x”025C”
0x»98”	0x”0260”
0x»99”	0x”0264”
0x»9A”	0x”0268”
0x»9B”	0x”026C”
0x»9C”	0x”0270”
0x»9D”	0x”0274”
0x»9E”	0x”0278”
0x»9F”	0x”027C”
0x»A0”	0x”0280”
0x»A1”	0x”0284”
0x»A2”	0x”0288”
0x»A3”	0x”028C”
0x»A4”	0x”0290”
0x»A5”	0x”0294”
0x»A6”	0x”0298”
0x»A7”	0x”029C”
0x»A8”	0x”02A0”
0x»A9”	0x”02A4”
0x»AA”	0x”02A8”
0x»AB”	0x”02AC”
0x»AC”	0x”02B0”
0x»AD”	0x”02B4”
0x»AE”	0x”02B8”
0x»AF”	0x”02BC”

Board Logical address	IT Address jump
0x»B0”	0x”02C0”
0x»B1”	0x”02C4”
0x»B2”	0x”02C8”
0x»B3”	0x”02CC”
0x»B4”	0x”02D0”
0x»B5”	0x”02D4”
0x»B6”	0x”02D8”
0x»B7”	0x”02DC”
0x»B8”	0x”02E0”
0x»B9”	0x”02E4”
0x»BA”	0x”02E8”
0x»BB”	0x”02EC”
0x»BC”	0x”02F0”
0x»BD”	0x”02F4”
0x»BE”	0x”02F8”
0x»BF”	0x”02FC”
0x»C0”	0x”0300”
0x»C1”	0x”0304”
0x»C2”	0x”0308”
0x»C3”	0x”030C”
0x»C4”	0x”0310”
0x»C5”	0x”0314”
0x»C6”	0x”0318”
0x»C7”	0x”031C”
0x»C8”	0x”0320”
0x»C9”	0x”0324”
0x»CA”	0x”0328”
0x»CB”	0x”032C”
0x»CC”	0x”0330”
0x»CD”	0x”0334”
0x»CE”	0x”0338”
0x»CF”	0x”033C”
0x»D0”	0x”0340”
0x»D1”	0x”0344”
0x»D2”	0x”0348”
0x»D3”	0x”034C”
0x»D4”	0x”0350”
0x»D5”	0x”0354”
0x»D6”	0x”0358”
0x»D7”	0x”035C”
0x»D8”	0x”0360”

Board Logical address	IT Address jump
0x»D9”	0x”0364”
0x»DA”	0x”0368”
0x»DB”	0x”036C”
0x»DC”	0x”0370”
0x»DD”	0x”0374”
0x»DE”	0x”0378”
0x»DF”	0x”037C”
0x»E0”	0x”0380”
0x»E1”	0x”0384”
0x»E2”	0x”0388”
0x»E3”	0x”038C”
0x»E4”	0x”0390”
0x»E5”	0x”0394”
0x»E6”	0x”0398”
0x»E7”	0x”039C”
0x»E8”	0x”03A0”
0x»E9”	0x”03A4”
0x»EA”	0x”03A8”
0x»EB”	0x”03AC”
0x»EC”	0x”03B0”
0x»ED”	0x”03B4”
0x»EE”	0x”03B8”
0x»EF”	0x”03BC”
0x»F0”	0x”03C0”
0x»F1”	0x”03C4”
0x»F2”	0x”03C8”
0x»F3”	0x”03CC”
0x»F4”	0x”03D0”
0x»F5”	0x”03D4”
0x»F6”	0x”03D8”
0x»F7”	0x”03DC”
0x»F8”	0x”03E0”
0x»F9”	0x”03E4”
0x»FA”	0x”03E8”
0x»FB”	0x”03EC”
0x»FC”	0x”03F0”
0x»FD”	0x”03F4”
0x»FE”	0x”03F8”
0x»FF”	0x”03FC”

Annex 25 : Board position



Modification

Version 1 : Initial Version

Version 2 :

Annex 21	Update
Etat register (VALCOM 170 pulses instead 340)	Update
Counter in circuit 7 (add explain for the VALID counter)	Update
Etat register (redefine the function of the ETAT6 bit)	Update
Annex 1 : Front end synoptic (redraw the ETAT6 signal)	Update
Assembly of the board (change some resistor value from 100 to 82,5 Ω)	Update
Add the CEDFPD_carte_fille board assembly subparagraph	Add
Front End definition	Update
CEDFPD_carte_fille board scheme	Add
CEDFPD board scheme	Add

Version 3 :

Grammatical and orthographical correction of the entire document	
Modify capacitor value on CI bottom view	Modify
Modify the “Figure 5: command counter sequencing” (p. 11)	Modify
Precision about User signals present on the VXI connectors (Chap. 6,p. 27)	Update
Update definition of the generation of the MC22 coincidence	Update
Update definition of the generation of the MF22 coincidence	Update

Version 4 :

Add Annex 24 : Interrupt vector address jump	Add
IT register description : add explain about interrupt vector	Update
Add chapter 4.1 Board addressing (determination of @base)	Add
Add chapter 4.1.1 Board logical address assignment	Add
Add Annex 25 : Board position , show the relative position of the different crate	Add

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